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EISCAT
TECHNICAL
NOTE

CORRELATOR BUFFER-MEMORY FOR THE EISCAT RADAR SYSTEM

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FOR

THE EISCAT RADAR SYSTEM

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SUMMARY

Correlator buffer-memory is a device which is going to be used as input data-area for the EISCAT digital correlator. It consists of two memory data-parts which can be addressed simultaneously. So, the loading of data to the buffer-memory and reading to the correlator are total independent of each other.

The buffer-memory has 8 program-counters which are programable from the computer. These counters are used for adressing while writing data from the filter and into the buffer.

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1.0 SPECIFICATIONS

Memory size: 32bit x 8k

Electrical Specifications: Power-Supply 40A, 5V

INPUT

Standard TTL-level inputs for address and data.

"1": 2.7 volts $\leq$ V out $\leq$ 5 Volts

"0": 0 volts $\leq$ V out $\leq$ 0.5 Volts

Input data-speed 10 MHz, with handshaking between CAMAC/buffer and matched filter/buffer. There is no handshaking between correlator and buffer.

OUTPUT

Standard TTL-level for all data outputs with 3-state.

IOL (sink current) = 64 mA

IOH (source current) = -15 mA

2.0 FUNCTIONAL DISCRIPTION

The buffer-memory is a divice which is going to be used as input-area for the correlator.
The memory is divided into two identical parts. The correlator has access to one part of the buffer-memory, while data are loaded into the other part from the filter. The write-addresses are generated in the buffer-control part, and the read addresses are generated by the correlator itself.
It is possible to connect one master and there slaves to one buffer-memory. And more than one buffer-memory may be connected to each matched filter. (Multi correlator system).
Block diagram is shown in figure 1.

2.1 MEMORY SYSTEM

The memory is divided into "pages" when one page is 1k word. Each memory-card consists of 1k x 32bit.
Extending the memory is done by adding more cards into the crate without doing any new handware design. The only thing to do is to set the card address in the crate by use of micro-switches on the memory-cards.

3.0 HOW TO DEVIDE THE BUFFER MEMORY

It is possible to divide the memory in different ways by programming the 8 programm-counters for input and enable databusses and paging for output by use of CAMAC.

3.1 INPUT

Each program-counter consists of a programable register and a 16 bit counter. So every counter can address the whole memory (4k). It is possible to divide the memory into channel-blocks by programming different start-addresses for each program-counter. One program-counter can address the area of another, so the addressing is very important. If only one frequency-channel from the filter is needed, program-counter 1 should be programmed with start-address 0, and the other with startaddresses greater than the address space.

All of the programcounters are cleared and reloaded with the start-addresses after each start-compute pulse from the radarcontroller. The programming of the counters is therefore necessary only once before starting up an experiment.

3.2 OUTPUT

There are 4 data-channels from the buffer-memory. Each of them consists of 16 bits. (8 bits for X-sample and 8 bits for y-sample). Where data shall flow are set by switches on the front-panel. (4 switches for each memory card). Each switch enables the wanted data-bus.

It is possible to divide the buffer-memory in many ways by use of the toggle-switches on the front and the tumble switches.

The thumble switches are used to divide the memory into blocks. The minimum size of one block is 1k word. So if we want to use one correlator and 3 slaves the minimum memory size is 4k. The start address for each block will be 0, so by use of 4 blocks one address from the correlator means data from 4 different places in the buffer-memory. The 4 different data-sets are sent to 4 different data-busses. (See fig. 2)

3.3. EXAMPLES FOR INPUT/OUTPUT

I.

One frequency-channel/ one correlator & no slaves.

This is the easiest configuration (fig. 2)

The upstarting procedure will be:

a) Program counter no 1 with start address

b) Connect and enable data-bus no 1 to all cards by use of computer

c) Set one block for output (whole memory) by use of computer

II.

8 frequency-channels/ one correlator and 3 slaves.

The upstarting procedure will be: (fig 3)

a) Program all program counters with start-addresses

b) Connect and enable each data-bus to the correct correlator and slave

c) Define blocksize for the correlator and slaves by using the computer

4.0 CONTROL SYSTEM (fig 1)

a) TIMING CONTROL gives the timing and anable signals to do it possible to write and read to/from the buffer-memory (fig 6 and 7)

b) DATA BUS CONTROLS control the 4 different data-buses of 16 bits each

c) CHANNEL CONTROLS control the program-counters and the programming of the counters (fig 8, 9 & 10)

d) DATA CORRECTION CONTROL makes all data sets usable for the correlator

4.1 TIMING CONTROL

Data strobe from the filter is used as time-reference for input to the buffer-memory. All control-signals are made by using data-strobe and start-compute. The start-compute signal is taken directly from the radar-controller.

A clear- and reload-pulse from this control is sent to the program-counters every time start-compute comes from the radar-controller. This means that all the program-counters are reloaded with the startaddresses after each start-compute and will be ready to count. The clock-pulse which steps the program-counters is generated at the same time as data-received is sent to the matched filter. Therefore will the new address be ready to the next load into the memory. The different enable signals are also generated in this control.

Input/output will change side of the buffer-memory after each start-compute.

4.2 DATA BUS CONTROLS

Each memory-card has its own data bus control which takes care of the enabling of the different databuses. Our enable-signal from the correlator does it possible to disable all the databuses at once, so the correlator can take data from other sources.

4.3 CHANNEL CONTROL

Consists of one part which controls the programming of the different program counters, and 8 channels controls which take care of the different program-counters for input to the buffer.

The program-counters have to be programmed through CAMAC. Each channel consists therefore of one input-register (16 bit programable), a 16 bit counter, and a 16 bit bus tranceiver. The tranceivers have 3-state outputs, so all channel-controls are linked to the same address bus.

4.4 DATA CORRECTION

Since the correlator cannot accept datawords which are -128_{10} this circuit is made. It adds +1 to the dataword for each x-y sample if the value is -128_{10}.

5.0 LOADING OF DATA

The channel-number (3 bit) is sent to the buffer from the matched filter together with the data. The channel-number is clocked into a 3-bit register, and changed to a decimal number. By gating this decimal output with data-received the clock-signal for the program-counters is made. One of the counters are now clocked forward one step so it is ready the next time when it is addressed.

The address-bus tranceivers are enabled or disabled by the signals E1A, E1B, E2A and E2B. Signal E1A = $\overline{\text{E1B}}$ so if tranceiver E1A is enabled is tranceiver E1B in 3-state. At the same time are E2A closed and E2B opened. The correlator can now get access to the other side of the memory. The data-bus tranceiver 3A has been opened earlier so data are now clocked into the memory. (See timing diagram fig 6).

5.2 READING FROM THE BUFFER

The correlator has direct access to the buffer through the tranceivers, and will therefore have to wait for the data. And no strobe signal or data-ready signal will be sent from the buffer to the correlator (no handshaking this way). (See timing diagram Fig 7).

5.3 PROGRAMMING

The programming from CAMAC is done by first setting up BUFFER NO. and which program-counter to be programmed. This is done in Register (The same module as for the correlator).
Register 2 is used as control and strobe of register 1 into the buffer-memory. Bit specifications on fig 4. Address/Dataflow between CAMAC and buffer memory on fig. 5. (See timing diagram fig 8, 9, 11).

6.0 INTERFACE

6.1 Buffer/Filter:

TTL standard is used.

"high level" : 2.7 Volt $\leq$ Vout $\leq$ 5 Volt

"low level" : 0 Volt $\leq$ Vout $\leq$ 0.5 Volt

The interface is organized on these buses:

a) Data-bus, 16 lines for transferring x,y-sample in parallel

b) Channel-bus, 3 lines for identification for channels

c) Control-bus, 2 lines for hand-shaking

Channel bus.

bit 2	bit 1	bit 0	Channel No.
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

6.2 INTERFACE

CAMAC/BUFFER

Figure 4 shows the interface between correlator/buffer and computer:

6.3 INTERFACE between

Buffer/Correlator

Linetranceivers will be used to drive the databuses from buffer to correlator. Balanced input/output is not used so the distance between buffer and correlator has to be very short. (Should be shorter than 2 m).

7.0 TESTING

Testing of the buffer-memory will be done by using CAMAC and the computer. There will be programs which simulates the match filters and the correlator. This will make it possible to test the buffer-memory in a dynamic way, but not at the highest working speed.

The address-buses for buffer A and buffer B are displayed on the front-panel, together with some other signals and status.

The bus-tranceivers which are used to buffer the databuses can be connected directly to CAMAC. So the output data-flow from the buffer may be tested through CAMAC.

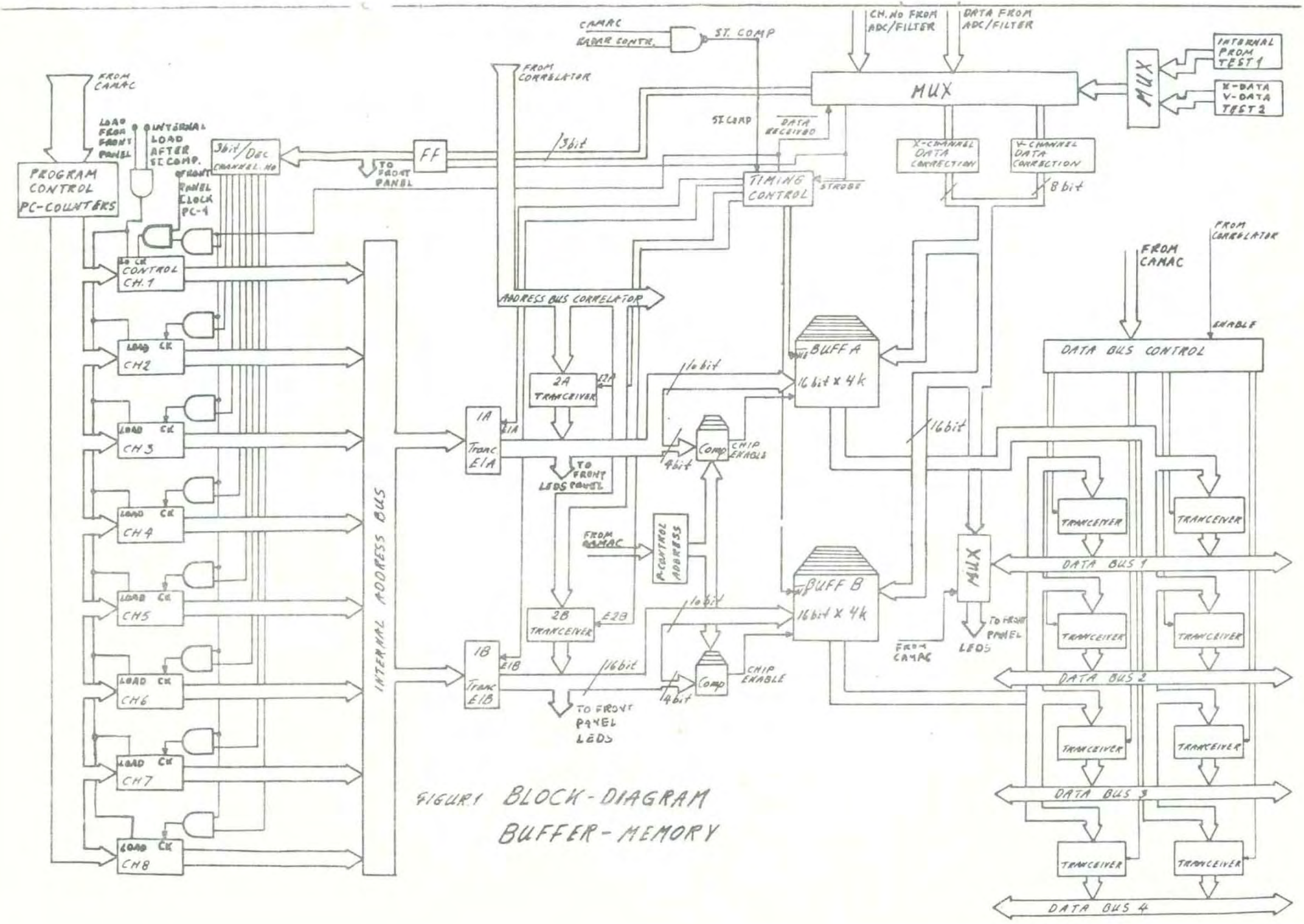
It will also be possible to use the buffer-memory as a buffer for the radar-controller. That means that the radar-controller may be tested with its normal speed.

7.1 Internal Prom

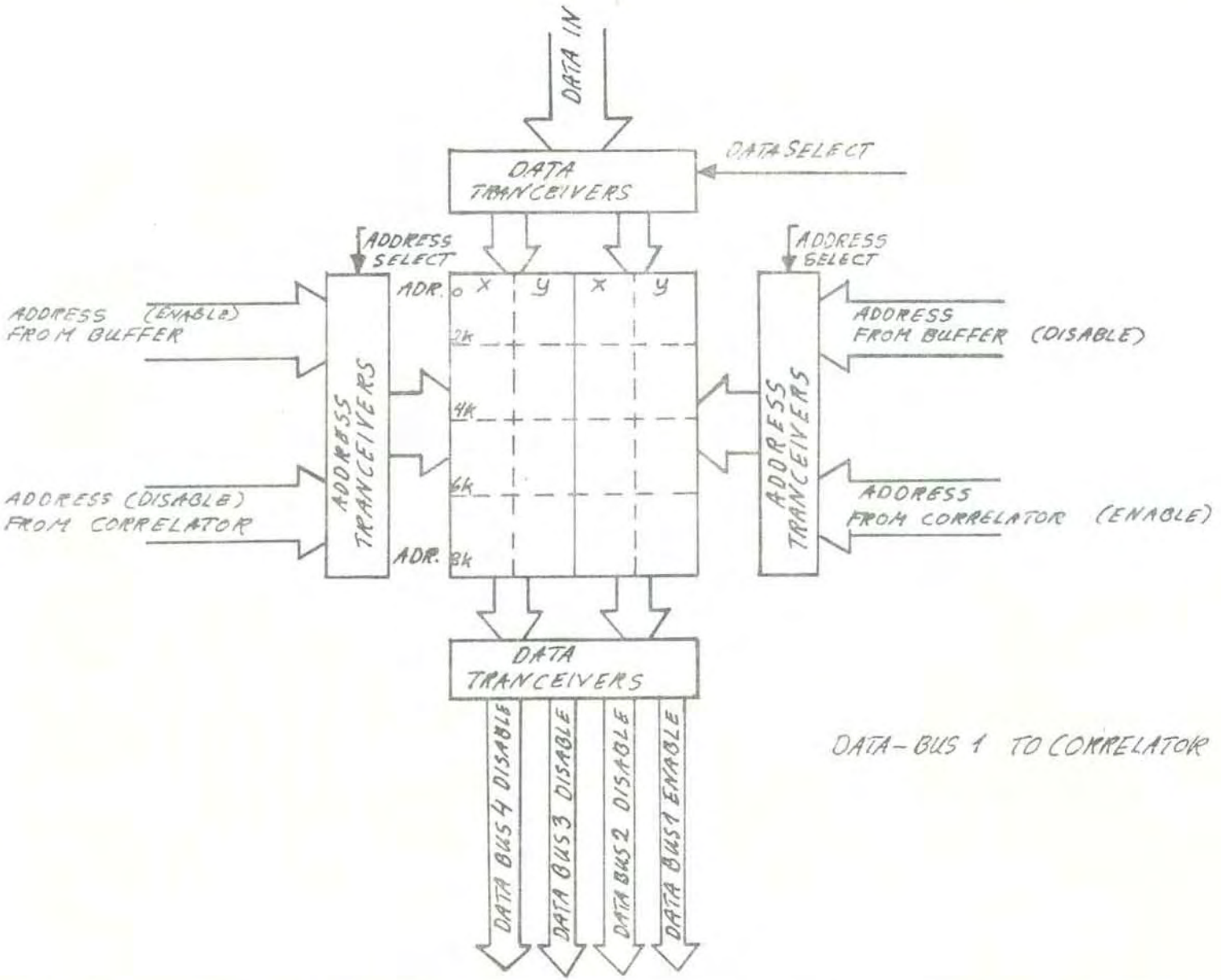
Testing (of both buffer memory and correlator) can be done by using the internal testprom in the buffer memory. X-data and Y-data are stored in (512 x 16 bit) prom, and data can be loaded into buffer from this prom.

7.2 X-data, Y-data

There is also a X-data, Y-data simulator which counts up for X-data and down for Y-data.
By using the tests which is described in 7.1 and 7.2 it is possible to do the testing in true speed, both for correlator and buffer memory.

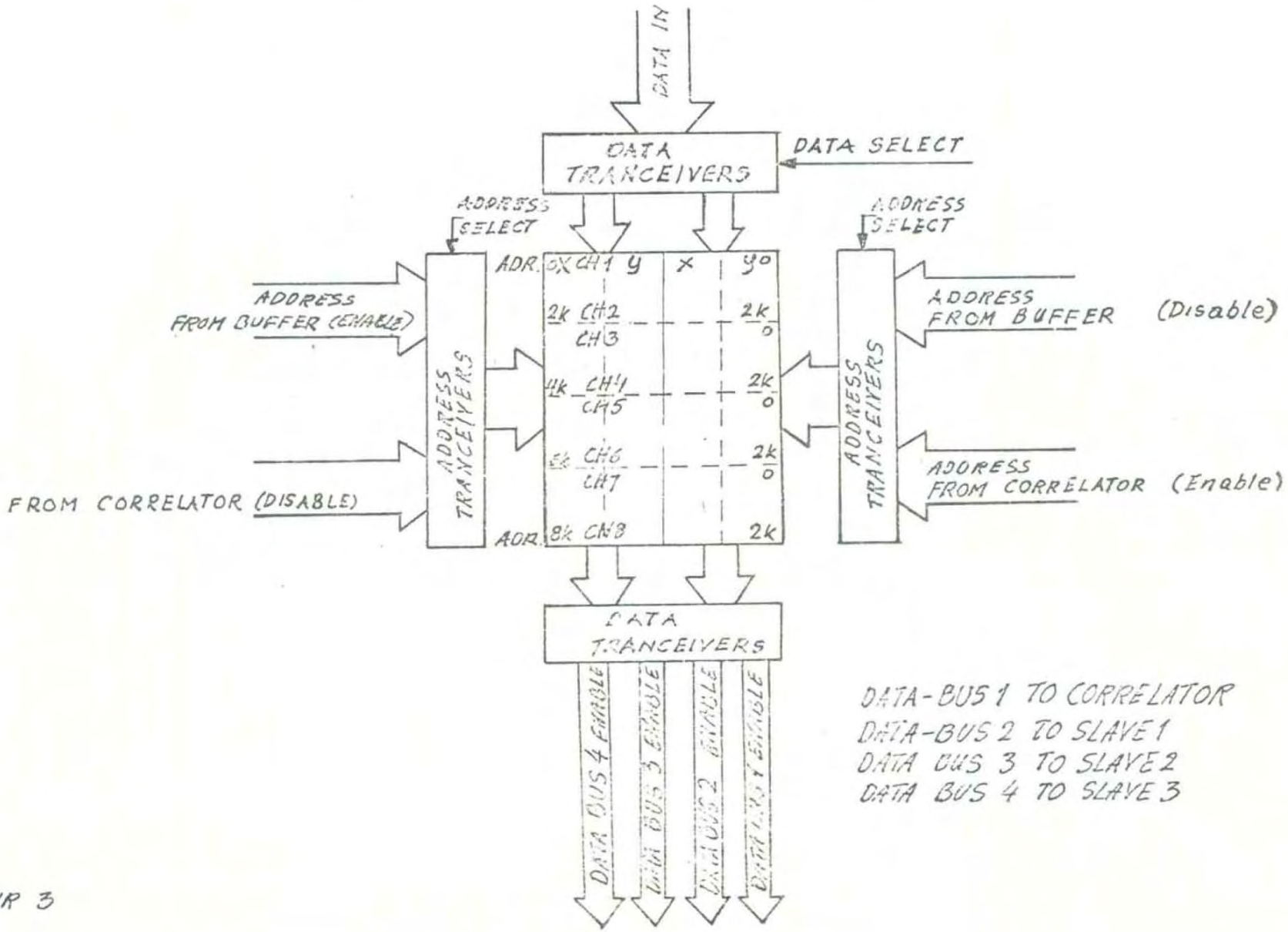


FIGUR 1 BLOCK-DIAGRAM BUFFER-MEMORY



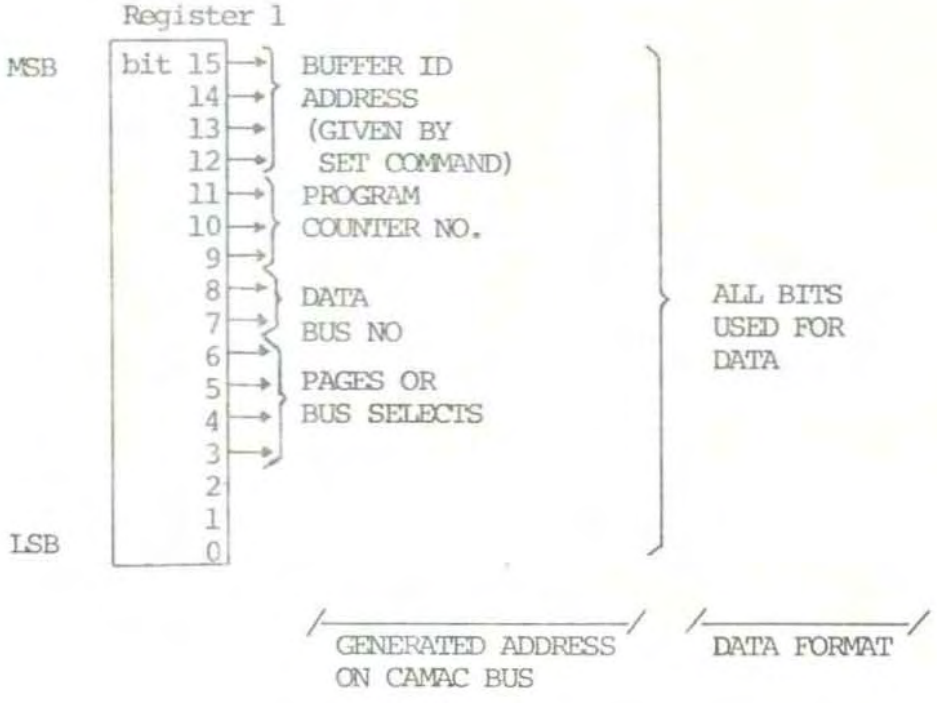
FIGUR 2

ORGANIZATION OF DATA BUSSES AND MEMORY. (1 channel and 1 correlator)



FIGUR 3

ORGANIZATION OF DATA BUSSES AND MEMORY (8 channels and 1 correlator / 3 slaves)



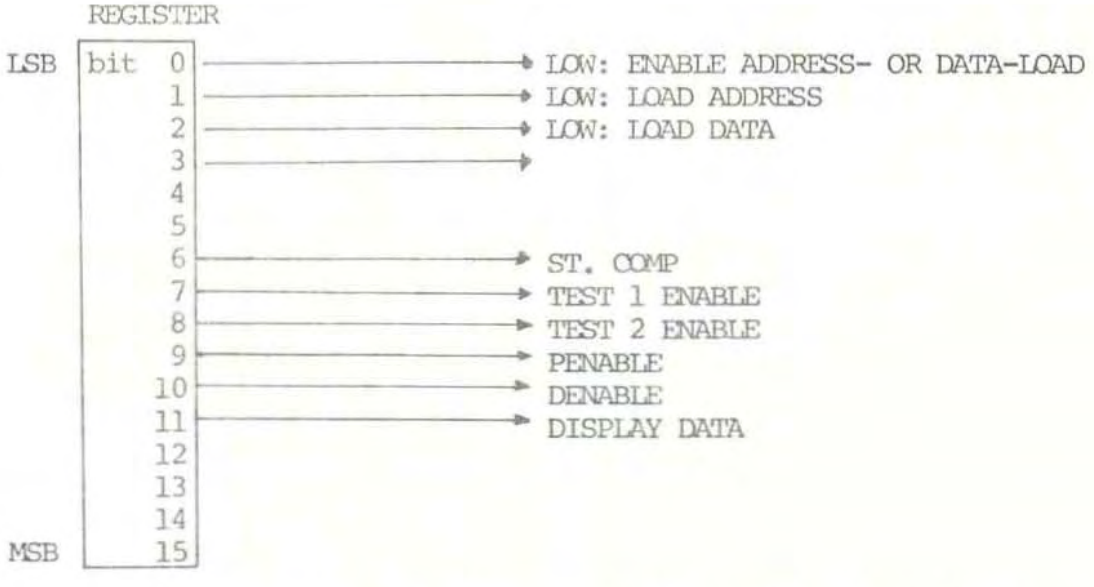


Figure 4. Correlator/Buffer Interface (Bit Specifications)

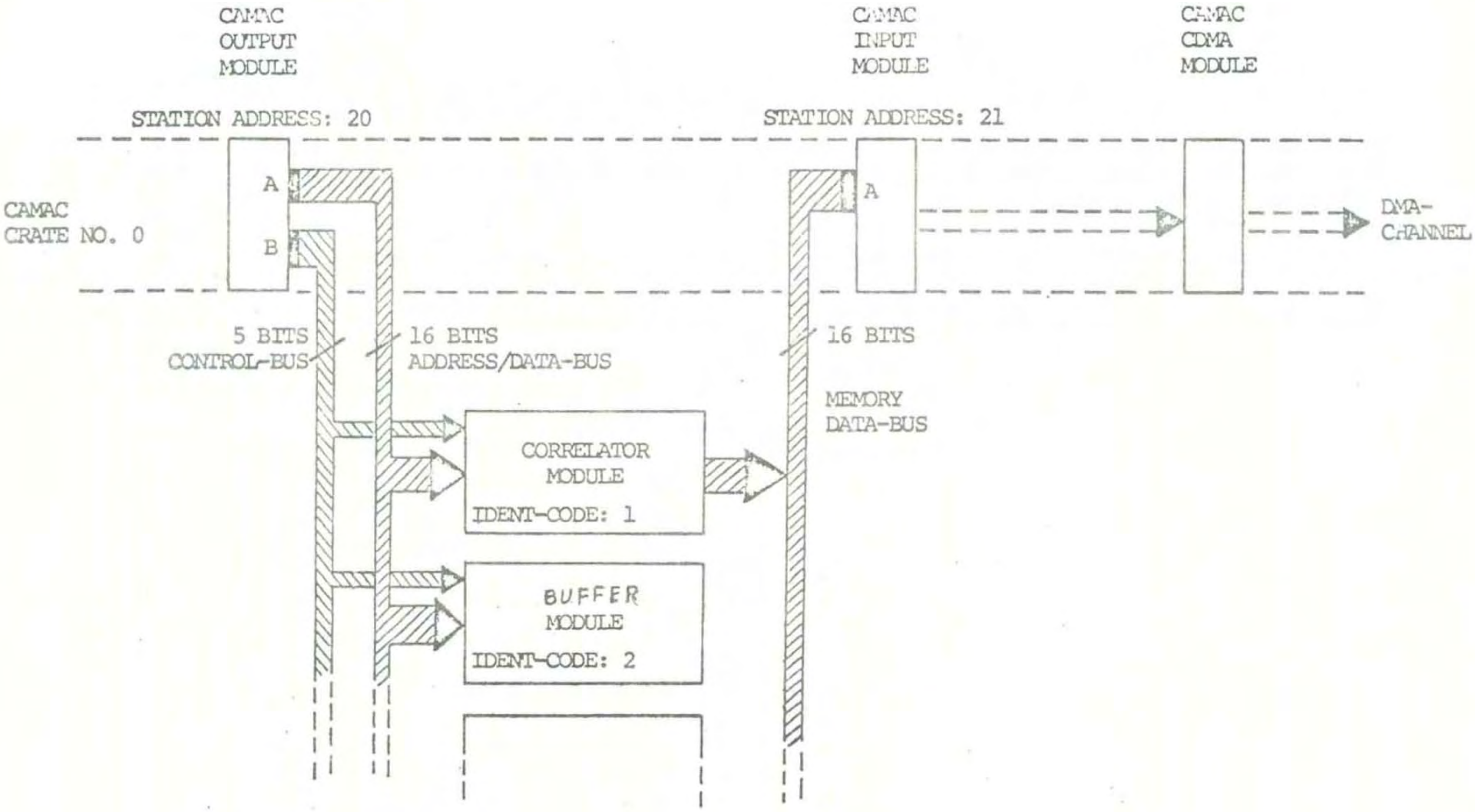


Figure 5. INTERFACE BETWEEN CORRELATOR SYSTEM AND COMPUTER.

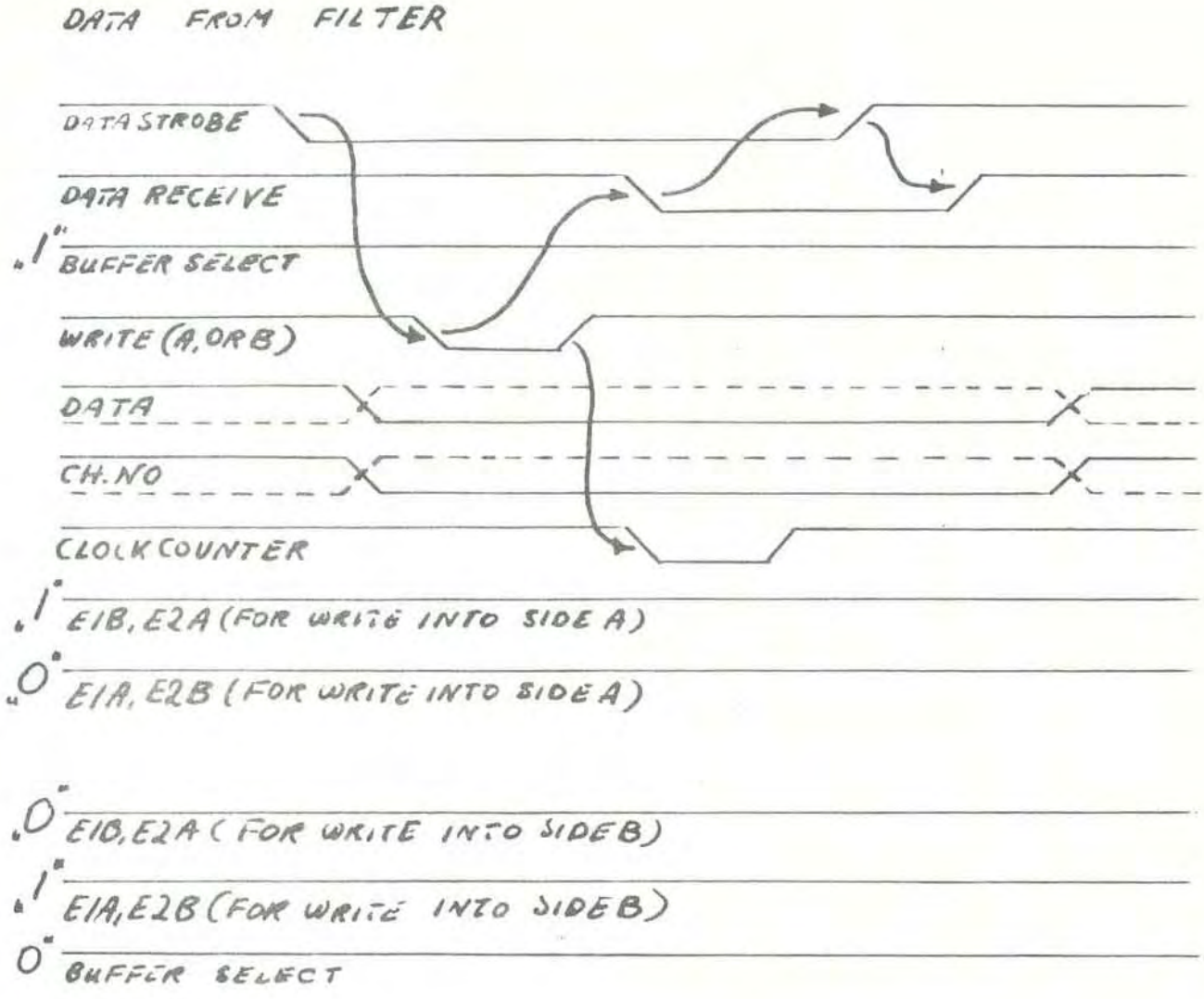

DATA FROM FILTER
DATA STROBE
DATA RECEIVE
"1" BUFFER SELECT
WRITE (A, OR B)
DATA
CH. NO
CLOCK COUNTER
"1" E1B, E2A (FOR WRITE INTO SIDE A)
"0" E1A, E2B (FOR WRITE INTO SIDE A)
"0" E1B, E2A (FOR WRITE INTO SIDE B)
"1" E1A, E2B (FOR WRITE INTO SIDE B)
0" BUFFER SELECT

fig. 6

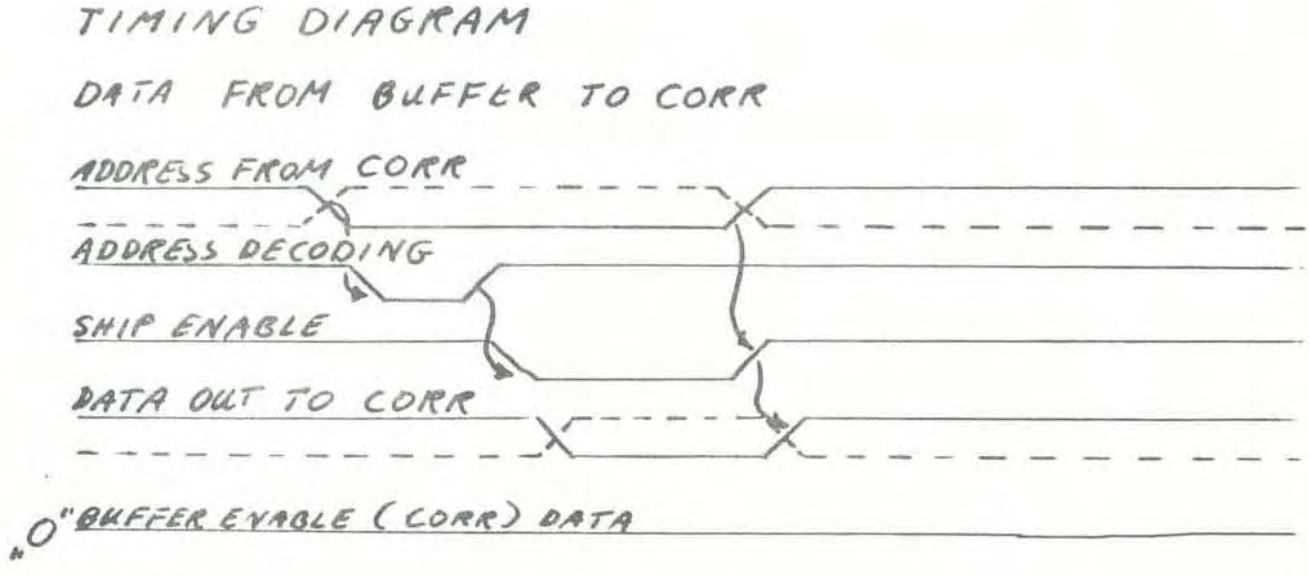

TIMING DIAGRAM
DATA FROM BUFFER TO CORR
ADDRESS FROM CORR
ADDRESS DECODING
SHIP ENABLE
DATA OUT TO CORR
"0" BUFFER ENABLE (CORR) DATA

fig. 7

TIMING DIAGRAM

PROGRAMMING OF PC-COUNTERS FROM CAMAC

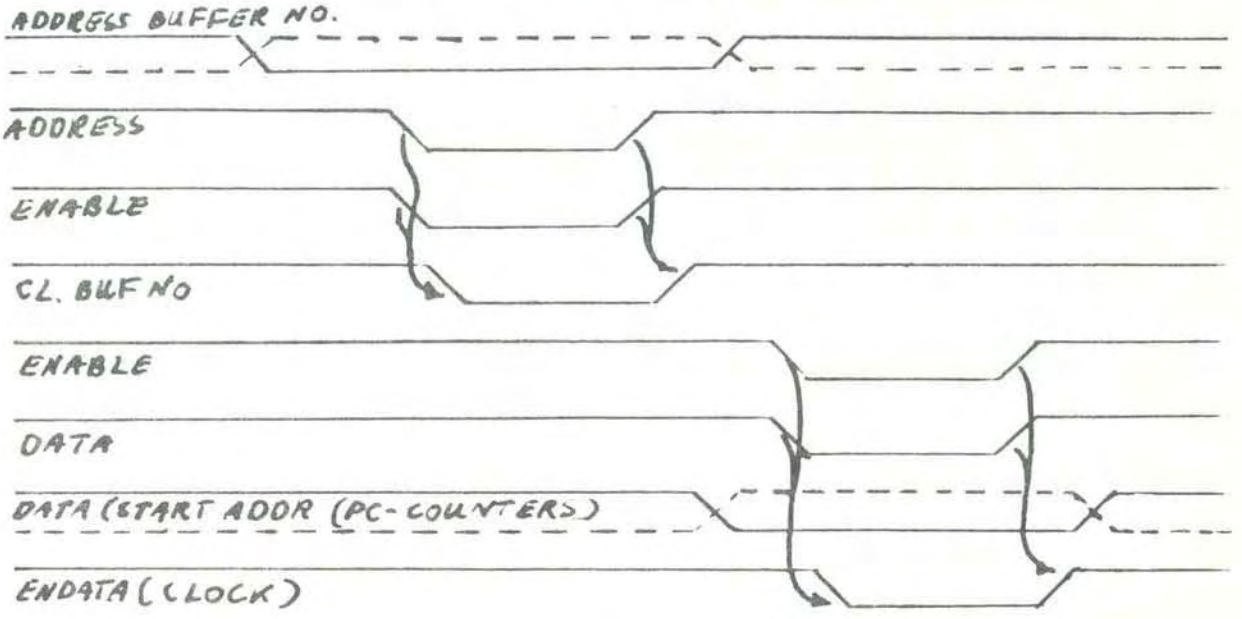


fig. 8

PROGRAMMING OF ALL PC-COUNTERS FROM CAMAC

FUNCTION TABLE

CH. NO BIT2	BIT1	BIT0	EN-DATA	CLOCK PULSES FOR PROGRAMMING ACK1	ACK2	ACK3	ACK4	ACK5	ACK6	ACK7	ACK8
0	0	0	⊓	⊓	⊔	⊔	⊔	⊔	⊔	⊔	⊔
0	0	1	⊓	⊔	⊓	⊔	⊔	⊔	⊔	⊔	⊔
0	1	0	⊓	⊔	⊔	⊓	⊔	⊔	⊔	⊔	⊔
0	1	1	⊓	⊔	⊔	⊔	⊓	⊔	⊔	⊔	⊔
1	0	0	⊓	⊔	⊔	⊔	⊔	⊓	⊔	⊔	⊔
1	0	1	⊓	⊔	⊔	⊔	⊔	⊔	⊓	⊔	⊔
1	1	0	⊓	⊔	⊔	⊔	⊔	⊔	⊔	⊓	⊔
1	1	1	⊓	⊔	⊔	⊔	⊔	⊔	⊔	⊔	⊓

fig. 9

COUNTING OF ALL PC-COUNTERS FROM ADC/FILTER

FUNCTION TABLE

CH. NO. Bit2	Bit1	Bit0	clock count	clock pulses for PC-counters PC-1	PC-2	PC-3	PC-4	PC-5	PC-6	PC-7	PC-8
0	0	0	⊓	⊓	⊔	⊔	⊔	⊔	⊔	⊔	⊔
0	0	1	⊓	⊔	⊓	⊔	⊔	⊔	⊔	⊔	⊔
0	1	0	⊓	⊔	⊔	⊓	⊔	⊔	⊔	⊔	⊔
0	1	1	⊓	⊔	⊔	⊔	⊓	⊔	⊔	⊔	⊔
1	0	0	⊓	⊔	⊔	⊔	⊔	⊓	⊔	⊔	⊔
1	0	1	⊓	⊔	⊔	⊔	⊔	⊔	⊓	⊔	⊔
1	1	0	⊓	⊔	⊔	⊔	⊔	⊔	⊔	⊓	⊔
1	1	1	⊓	⊔	⊔	⊔	⊔	⊔	⊔	⊔	⊓

fig. 10

TIMING DIAGRAM

PROGRAMMING PAGING AND DATABUS ENABLE FROM CAMAC

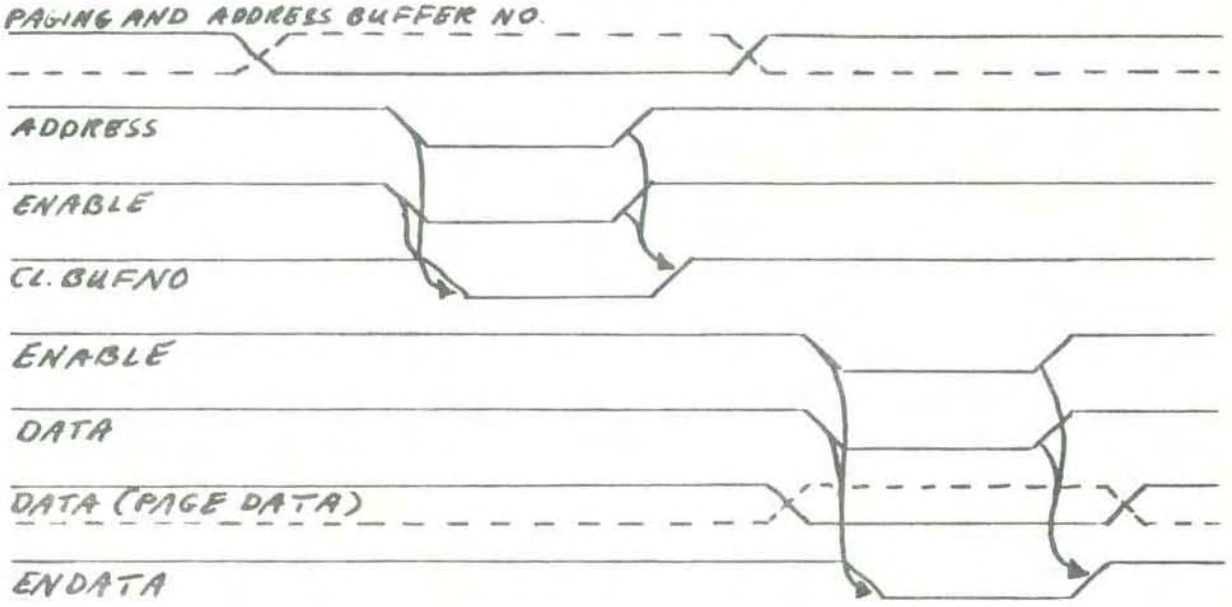


fig. 11

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