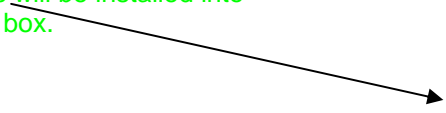


The descriptions of the bits of the RC memory row (32+6 bits) of the E3D-demonstrator-radar controller

Bit N:o	Signal	Direction	Description	Destination
	LPRPint		Not programmable	
61	Spare			
60	Spare			
59	Spare			
58	Spare			
57	Spare			
56	Spare			
31	Rx-sync			
30	EN_data 6	O, neg. active	Dis/enables input data flow of the Chan. board 6	Data driver 6
29	EN_data 5	O, neg. active	Dis/enables input data flow of the Chan. board 5	Data driver 5
28	EN_data 4	O, neg. active	Dis/enables input data flow of the Chan. board 4	Data driver 4
27	EN_data 3	O, neg. active	Dis/enables input data flow of the Chan. board 3	Data driver 3
26	EN_data 2	O, neg. active	Dis/enables input data flow of the Chan. board 2	Data driver 2
25	EN_data 1	O, neg. active	Dis/enables input data flow of the Chan. board 1	Data driver 1
24	Spare			
23	SIGINJ	O, ?	Test signal injection	Front-end LNA/ADC
22	SampG	O, neg. active	Sample gate for the DDC input	DDC
21	SYNCIN	O, pos. pulse	Synchronization clock for the DDC	DDC
20	(Start	O, ?	Frame counter start pulse	Frame counter)
19	Spare			
18	Spare			
17	Bufflip	O, neg. pulse	Changes the role of buffer memory sides	Channel boards
16	Spare			
15	CHON 6	O, neg. active	Dis/enables data writing into the BM 6	Channel board 6
14	CHON 5	O, neg. active	Dis/enables data writing into the BM 5	Channel board 5
13	CHON 4	O, neg. active	Dis/enables data writing into the BM 4	Channel board 4
12	CHON 3	O, neg. active	Dis/enables data writing into the BM 3	Channel board 3
11	CHON 2	O, neg. active	Dis/enables data writing into the BM 2	Channel board 2
10	CHON 1	O, neg. active	Dis/enables data writing into the BM 1	Channel board 1
9	Spare			
8	INT	O, pos. pulse	Interrupt to DSP	CH-adapter board
7	Spare			
6	Spare(CH7)	O, neg active	Can be used to CHON 7 if needed	
5	Spare			
4	Spare			
3	S3	Output	Status bit 3 to DSP interface boards	CH-adapter board
2	S2	Output	Status bit 2 to DSP interface boards	CH-adapter board
1	S1	Output	Status bit 1 to DSP interface boards	CH-adapter board
0	S0	Output	Status bit 0 to DSP interface boards	CH-adapter board
	PatchClk *)	O, pos. pulse	Strobes the RC register, on CH-adapter board	
	LPRPint		Last Pulse Repetition Period interrupt from R/C HW	
	PatchClk		Timing Clock, from R/C HW	
	Running		R/C running, from R/C HW	

Green NEW!  
Data drivers will be installed into the SerDes box.



1) Pins are defined in the RC pin assignment document (rows P2 a1-a32 and P2 c1- c32).  
\*) Separate signal from the RC.