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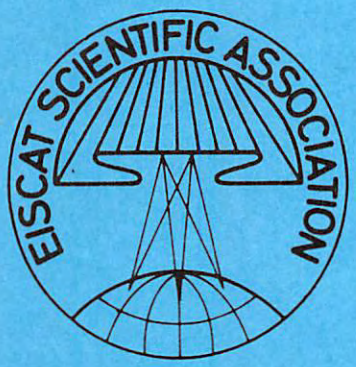

EISCAT
TECHNICAL
NOTE

SPECTRUM ANALYZER

by
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EISCAT Technical Note 83/39

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1. INTRODUCTION

In this report, a real time spectrum analyzer designed at the EISCAT Sodankylä site is described. This report is a short version of the original report on the analyzer.

This short report has been written because the original one was written in Finnish which probably discourages anybody not understanding that strange language from reading it.

The spectrum analyzer was designed especially for plasma line analysis. The design work was started when an interesting component, a charge coupled device (CCD) made by Reticon, became available. That CCD is designed to make Fourier transforms at relatively high speed.

The CCD chip does a convolution which can be used with the chirp z-transform algorithm to compute a discrete Fourier transform (DFT). The chip has 512 stages which means that it can be used to make a 512 point DFT. The maximum sampling rate of the CCD is 2 MHz; but in the constructed spectrum analyzer, a one MHz rate is used. This is mainly because higher speed readout circuits for the CCD were difficult to obtain.

Thus at one MHz sampling rate, the analyzer makes one DFT in 0.5 ms in the continuous mode when a so-called sliding DFT is made. When the data is recycled to make a normal DFT, it takes 1.0 ms to get a 512 point DFT. Thus the maximum continuous sampling rate of the analyzer in recycling mode is about 500 kHz. In this mode it is also possible to analyze and integrate non-stationary signals because the analyzer includes an input buffer memory which can be triggered externally to sample data.

In the next chapter there is some discussion on spectrum analysis and then in the following chapter the design and construction of the analyzer is described.

2. ON SPECTRUM ANALYSIS

2.1 GENERAL

The estimation of power spectrum has long been based on computing Fourier transforms, especially since the development of the Fast Fourier Transform algorithm (FFT). In this method, there are some disadvantages, like poor frequency resolution and high sidelobes. These features are most prominent when the data vector which is transformed is short.

The high sidelobes are related to the windowing of the data. When the FFT is applied it is implicitly done using a rectangular window which truncates the data set and supposes that the data is zero outside the transformed set. To avoid that problem, several window functions have been developed; but these decrease the frequency resolution and might increase the variance in some cases.

To solve these problems, some new methods for spectral estimation have recently been developed. These are called parametric methods because in them a model is made for the target and the parameters of that models are then estimated. These new methods are discussed in references 4, 5 and 32.

The advantage of the new estimation methods is that it is possible to get reliable results from short data sets. The disadvantage is that these methods need longer computation times than the traditional FFT algorithm and thus they are not normally applicable for real time processing.

Thus the spectrum analyzer developed for EISCAT is also based on a Fourier transform computation; in this case the algorithm used is the chirp z-transform instead of the FFT.

2.2. THE DISCRETE FOURIER TRANSFORM

The discrete Fourier transform (DFT) is defined:

$$X(k) = \sum_{n=o}^{N-1} x(n)W^{kn}, \quad k=0,1,\ldots N-1 \qquad (1)$$

where

$$W = e^{-i(2\pi/N)} \qquad (2)$$

In these formulae N is the number of samples, x(n) is a sample in time space and X(k) is a transformed point.

The discrete Fourier transform has a period N and if an inverse transform is made, the time series is then also periodic. This indicates that the Fourier transform distorts a continuous signal into a periodic one.

When the DFT is used for spectral estimation, the process to be analyzed is normally stationary and ergodic. Then it is possible to use time averages to estimate the statistical properties of signal.

The power spectrum comes from the DFT by formula:

$$S(k) = \left| 1/N\ X(k) \right|^2. \qquad (3)$$

This power spectrum estimate is also called a periodogram.

If a spectrum estimate is computed using the above formula, the result may be statistically rather unreliable. Although the number of samples is increased, the variance of the estimate does not decrease when the signal is white noise (ref. 6). This indicates that to decrease the variance, an average of several estimates must be computed. Another possibility is to use a window in the frequency domain.

2.3 THE CHIRP Z-TRANSFORM

The basic idea of the chirp z-transform (CZT) is to use a convolution to perform most of the calculations which are needed in the DFT. The CZT algorithm can be derived from formula (1) by substitution:

$$nk = (n^2 + k^2 - (k-n)^2)/2 \qquad (4)$$

This gives:

$$X(k) = e^{-i\pi k^2/N} \sum_{n=0}^{N=1} (x(n)\, e^{-i\pi n^2/N})e^{i\pi(k-n)^2/N}, \qquad (5)$$

$$k = 0,1,\ldots,N-1.$$

This can be handled as a three phase process where first a new data series is made:

$$y(n) = x(n)W^{n^2/2}, \quad n = 0,1,\ldots,N-1. \qquad (6)$$

Then a convolution is made between y(n) and v(n) where v(n) is:

$$v(n) = W^{n^2/2}. \qquad (7)$$

This gives a sequence:

$$g(k) = \sum_{n=0}^{N-1} y(n)v(k-n), \quad k = 0,1,\ldots,M-1 \qquad (8)$$

The third step is to multiply g(k) by sequence $W^{k^2/2}$:

$$X(k) = g(k)W^{k^2/2}, \quad k = 0,1,\ldots,M-1. \qquad (9)$$

The sequence (7) is a complex sinusoidal function where the frequency increases linearly. That is called chirp. From the formulas above it can be seen that the number of transformed points in CZT need not to be the same as the number of data points in general case.

When the charge coupled device is used to compute the CZT it is phase two described by formula (8) which is done by the CCD. This means that the chip does most of the calculations which are needed to compute the DFT.

When the power spectrum is computed using the CZT, it is possible to omit the last factor because the magnitude of that factor is always one and it affects only the phase. Thus the final formula for the power spectrum estimastion by CZT is:

$$\left| X(k) \right|^2 = \left| \sum_{n=0}^{N-1} (x(n)\, e^{-i\pi n^2/N})\, e^{i\pi(k-n)^2/N} \right|^2 \quad . \qquad (10)$$

3. OPERATION OF THE SPECTRUM ANALYZER

3.1 INTRODUCTION

A block diagram of the spectrum analyzer is given in fig.1. The complex samples from the ADC are first read into the buffer memory of the spectrum analyzer. The buffer memory is divided into two parts; when one side of the memory is written, the other side is read.

From the buffer memory the data is read into four multipliers, which are needed in the chirp z-algorithm. The other multiplicants come from the chirp ROM chips. From the multipliers the data go to arithmetic logic units (ALUs), which perform addition and subtraction according to the algorithm. Then the data are transformed to analog form for the CCD.

The CCD chip is controlled by one megaherz clocks. This means that the sampling rate of the CCD is also 1 MHz. The data is read out from the CCD by buffer amplifiers and then it is fed to differential amplifiers to extract the data from the CCD clock lines 1 and 3.

The voltage coming out from the differential amplifiers is digitized by fast flash ADCs. Then the spectral components are squared and summed to get the power spectrum. Because the points of the power spectrum are coming out from the CCD in serial, the rest of the system also runs at 1 MHz rate.

The integrator has four 512 point memory banks, 32 bits wide. The integrated results are written simultaneously to the integration memory and to the read-out memory. When the integration period ends, DMA starts from the read-out memory and a new period is started in the integration memory after first reseting it.

There is also a display controller in the spectrum analyzer which can be used to show the spectra on an oscilloscope screen. The display controller contains an automatic scaler which always shows the 8 highest used bits in the spectra. Manual scaling is also possible.

Start and stop command for the analyzer can be given either manually or from the computer. Also the integration time can be controlled from the radar controller or internally by the spectrum analyzer.

3.2 TIMING ARRANGEMENT

The basic timing of the spectrum analyzer is based on a 16 MHz crystal controlled oscillator. Fig.2 shows the clock generator circuit diagram. The 16 MHz signal goes to a counter which controls two decoder chips. These decoders are four-to-sixteen and three-to-eight devices which then generate sixteen 62.5ns pulses C0...C15 and eight 125ns pulses S0...S7, respectively, during a microsecond. These pulses are used to control the synchronous part of the spectrum analyzer.

The data write phase into the buffer memory is controlled externally by the data strobe signal coming from the ADC. Thus writing is asynchronous compared to the other part of the system.

At the user level, the timing of the analyzer is controlled by the desired integration time. With no integration, a normal DFT spectrum can be obtained every millisecond.

3.3 BUFFER MEMORY AND PREMULTIPLIERS

Fig.3 is a circuit diagram of the buffer memory. The data which come from the ADC (2 x 8 data bits + 3 address bits) are divided into two independent busses which allow simultaneous write and read phases in the memory. The three address bits which come with the data are compared in a channel selector to allow only data coming from one channel to be strobed into the memory. It is possible also to switch the channel selector.

Fig.4 is a timing diagram of the buffer memory write and also the buffer memory read synchronization. The operation of the buffer memory is controlled by the control flip-flop (fig.3). When the operation starts, this FF is cleared and the first data words are written into memory side one. After 512 words are written the address counter of side one generates a flip buffer signal which toggles the FF and enables writing into the other half of the memory.

The flip buffer signal also starts the synchronization of the read phase of the buffer memory (fig.4) and thus enables the reading. The two FFs, FF1 and FF2, are used to synchronize the reading.

In the recycle mode which is used in the spectrum analyzer the buffer memory must be read twice for each data set. For this purpose a recycle FF (fig.3) is included in the buffer memory control part. During the first cycle, data is read to the CCD and then during the second reading cycle integration is done.

When the clock rate of the analyzer is 1 MHz, the maximum writing rate into the buffer memory is about 500 kHz. If this rate is exceeded, an error occurs that is indicated by an input error FF driving an error LED on the front panel of the analyzer.

In the chirp z-algorithm the data must be multiplied by sine and cosine chirp functions. These functions are stored in 512 x 8 bits ROMs. These ROMs are read synchronously with the data from the buffer memory; the address counter of the ROMs is clocked by clock pulse SO.

Before reading the data from the ROMs into the multipliers a modification is done which converts the value -128 to -127 because the multipliers used can not handle multiplication -128 x -128. The ROM address counters and the modification circuits are shown in fig. 5.

Fig.6 is a circuit diagram of the arithmetic part. First the data and the chirp functions are read to multipliers which are TRW MPY-8HJ chips. The data and chirp functions are in two's complement format. The additions and subtractions which are needed in the algorithm are performed by AMD 25LS2517 ICs. The timing of the premultipliers is shown in fig. 7.

3.4 CONTROL AND READOUT OF THE CCD

The Reticon charge-coupled device, R 5601 is controlled by a four-phase clock. The timing of these four clock signals is given in figure 8. In the same figure there is also the timing of the C(i) and S(i) pulses, which are used to generate the phi-pulses ($\Phi_{1,2,...}$).

The circuit diagram of the clock drivers of the R 5601 is shown in fig. 9. The four main clock lines, phi 1...4, are highly capacitive; phi 1 and 3, are about 500 pf, and phi 2 and 4 are about 200 pf. Because the required voltage level of the pulses is 10-14 volts, special driver circuitry is needed to avoid over- and under-shoots as much as possible. After testing several different solutions, the one given in fig. 9 turned out to be the best and was adopted.

In this system the TTL level clock signals first control driver circuits DS 0026. These ICs then drive n-channel FETs which are the final driver transistors. The supply voltage of the DS 0026 chips is 22 volts for clocks 1 and 3 and it is dropped to 20 volts for the FETs. This gives pulses of about 12 volt for the clock lines. For lines 2 and 4 only about 5 volts are needed. It is important to filter carefully the voltage lines for the main clocks.

The other control clocks for the CCD are driven by CMOS gates wich are supplied by 15 volts. These gates are driven by TTL open collector circuits.

In fig. 10 there is a schematic illustration of the charge transfer in the CCD together with the phi-pulse timing which was given in fig.8.

The signal processing circuits which are needed with the CCD are given in fig.11. These components and the driver circuits in fig.9 are located on one double european printed circuit board.

The data comes first to the DACs (TRW TDC 1016) The analog voltage is then amplified and shifted to about 6 volt level where the maximum signal amplitude is about 4 volts. The settling time of the DACs to 0.1% is 25ns and that of the MSK 730 amplifiers is 100ns.

The convolution made by the CCD is read out from the main clock lines phi 1 and 3. This is done in principle by a differential amplifier which reads the phi (+) and phi (-) lines.

To reduce the swing of the clock lines before the differential amplifier there is first a capacitive divider and also CMOS switches to reset the lines between the pulses. Then there are buffer amplifiers (LH 0033) to get equal impedances for the clock lines. The differential amplifier is a LH 0032 type which has a settling time of 300ns to 0.1%. The amplification is set to 25 to get about a 10 volt maximum output for the ADC.

In the readout circuit of the CCD there is an offset compensation system. This is described in fig.12 and in fig.11. The ADC is used in two's complement mode and thus the sign bit always tells whether the output voltage of the differential amplifier is positive or negative. That sign bit is used to control an integrator which in turn controls the offset voltage of the other buffer amplifiers. Thus the compensation system takes care of all offset voltages within the feedback loop. The maximum output voltage swing from the offset compensation circuit is about +/- 15 volts which is then attenuated down to +/- 15 mV for the buffer amplifier.

The ADC, a TRW type TDC 1007, is an eight bit flash converter. The timing of the readout system is shown in fig.7.

The offset compensation circuit tends to generate some noise when there is no signal to be analyzed in the device because operating the system always generates changes in the sign bit. This means that the ADC output varies between 0 and -1 even when there is no signal coming from the CCD. When there is a signal to be analyzed in the system this is not a problem with reasonable integration periods.

3.5 POWER COMPUTATION AND INTEGRATION

If Fourier coefficients are needed, then the signal coming from the CCD must be post-multiplied by a chirp factor. But if only the power spectrum is needed, then no post-multiplication is necessary since phase information is irrelevant when computing power spectra.

The power computation is done by the circuit given in fig.13. The data from the ADC first comes to multipliers (TRW MPY-8HJ) where the real and imaginary parts are squared and the squares added together to get power. There is also a DAC to display the eight most significant bits of the data for test purposes.

After the power computation, the data go to the integrator. This is shown in fig.14. There are eight 4-bit ALUs which add the computed power to the previous data from the integrator memory. ALU units are used to permit writing of zeroes into the memory before starting a new integration period. After adding, the data is stored in registers and then written into the integrator memory.

The integrator memory is made of eight Mostek MK 4118 1K x 8 bit chips which are configured to provide four 512 x 32 bit integration banks. The number of banks is selected externally by a switch on the front panel of the analyzer. The address counter is used to control the amount of banks as described in fig.14. The timing of the integrator is given in fig. 15.

The operation of the integrator is controlled by the circuit shown in fig. 16. The enable integration signal coming from the buffer memory is used to set a FF which controls multiplexer circuits that drives the integrator control signals. The timing of the integrator control is shown in fig.17. Also shown is the timing for the start of a new integration period when there is a memory clear cycle before the integration cycle. When integration takes place into four banks, four Enable Memory clear pulses are needed.

The integration period is controlled by a counter shown in fig.18. The counter is made up of 6 up/down counter chips which count the integration cycle complete (ICC) pulses coming from the integrator. The counters are preloaded at the beginning of the integration period from the registers which contain the number of cycles to be integrated. That register is loaded manually from front panel switches.

It is also possible to control the integration time externally from the radar controller. That option is selected by a manual switch from the front panel and it controls the operation of a multiplexer as described in fig.16. For the DT pulse coming from the radar controller there is an additional delay of about 1.5 seconds to allow parallel operation of the spectrum analyzer and correlator.

Fig.19 is a delay diagram for the spectrum analyzer that shows the pipe-line delay in the system. From the figure it can be seen that in addition to the 512 microsecond delay caused by the CCD there is a three microsecond delay. This is taken into account by the pipe-line delay counter shown in fig.16. The counter is needed to arrange the integration timing such that all data points for a CZT are taken from one data set. This is important when several spectra are integrated simultaneously.

3.6 DISPLAY AND OUTPUT CONTROL

When the integration period has finished, the data is transferred by DMA into the computer. To make the transfer without disturbing the operation of the analyzer, a special output memory has been included in the system.

When the integration is running this output memory is written in parallel with the actual integration memory. When the integration period ends, the DMA is started from the output memory and a new integration period is started simultaneously. When the data transfer into the computer has finished the output memory starts to operate in parallel with the integration memory again. This means that, in principle, there is almost the entire integration period for data transfer; only one parallel integration cycle is needed to update the output memory.

The circuit diagram of the output memory is given in fig.20. The A-bus from the integrator comes to the readout part of the system where there is a tri-directional bus driver which transfers the data into the output memory and to the display system. The DMA system described in fig. 20 is intended for an interface which has no handshake system. There the trigger DMA pulse is used to control the timing of the DMA. Another system has also been designed where a handshake with the input module in the computer (or CAMAC) can be used. For the DMA interface, the 32 bit wide data words are multiplexed into a 16 bit bus to make the system compatible with the ND-10 computer.

The display controller is described in fig.21. There the C-bus coming from the output memory goes to a multiplexer which takes 8 bits for the display ADC. The multiplexer can be controlled either manually or automatically. In automatic mode, the multiplexer takes the 8 highest used bits from the bus. This results in a continuous optimum scaling of the display during integration.

3.7 CONTROL OF THE SPECTRUM ANALYZER

The operation of the spectrum analyzer can be controlled either manually from the front panel or by computer. The control part of the system is shown in fig.22. A multiplexer, controlled from the front panel, selects either manual or computer mode for the analyzer.

To initialize the analyzer, a clear/load command must be given to the analyzer. Then the run command can be given and the analyzer goes from the STOP state into the READY state where it waits for the first data strobe signal. When that comes, it sets the analyzer to RUN state until it is stopped again. This means that there is no upper time limit between the data strobe pulses which are coming into the device. Thus the sampling rate can be as low as desired.

The interface of the spectrum analyzer with the EISCAT receiving system is shown in fig.23.

4. SPECTRUM ANALYZER TESTS

4.1 ON THE ANALYSIS OF THE TEST RESULTS

The spectrum analyzer has been tested in two basic ways. First it was used in the test mode to measure the integrated noise generated by the spectrum analyzer itself. Then external noise from the receiver has been analyzed and integrated, and the variance of the integrated spectrum compared to the theoretically expected value.

It can be shown that the variance of integrated spectra can be computed by the formula:

$$\mathrm{var}\left(\sum_{i=1}^{N} S_i\right) = 1/N\left(E(S_N)\right)^2 \qquad (11)$$

where N is the number of added spectra, S_i are the spectra to be added and S_N is the sum of spectra. Thus the formula says that the variance of the integrated spectra is equal to the square of the expectation value of the sum divided by the number of added spectra.

This indicates that it is possible to reduce the variance of a spectrum estimate by integration.

The theoretical result of formula (11) has been used to compare to the experimental variance of integrated spectra. It must be noted that generally the variance of a spectrum means the variance of one spectral point of different spectra. This makes the variance a function of frequency as it is in general case (ref.6,7,32). When (11) was used with spectrum analyzer tests, the variance was calculated from one integrated estimate normally over 200 spectral points. Thus the variance within a spectrum was analyzed to see if there are differences between the spectral channels in gain or noise.

4.2 TEST RESULTS

The dynamic range of the spectrum analyzer was computed from the test measurements when test mode and noise input was used. In ref.27, it was informed that the dynamic range of the CCD is specified to be 60 dB. This is defined to be the ratio of the peak output signal to the rms noise. In tests the noise generated by the system was measured by integrating it and then calculating the rms average noise in one channel.

The dynamic range of the CCD can be calculated by

$$DYN = V_{pp}/V_N \qquad (12)$$

where V_{pp} is the maximum peak-to-peak amplitude of one CCD output signal and V_N is the average RMS noise of that output. The RMS noise can be calculated by the formula:

$$V_N = V_{LSB} \sqrt{((S_N)/N)/2} \qquad (13)$$

where V_{LSB} is the amplitude represented by the LSB of the ADC, S_N is the average value of the integrated spectrum and N is the number of integrated spectra.

When V_{pp} is +/- 5V, V_{LSB} is +/- 5mV, N is 1.4×10^5 and S_N is 1.56×10^5 as in fig. 24, the dynamic range is 62.5 dB. The results were within +/- one dB with different values of N.

When external receiver noise was used to test the device, formula (11) was used to evaluate the results. Shown in fig.25 are four spectra of filtered noise. The number of spectra integrated are 10, 100, 1000 and 10 000. The decrease of the variance with increasing N is clearly shown in the figure.

From the results it can be seen that the variance of the first three spectra agree well with the variance calculated by formula (11). When N is 10^4, the measured variance is about 50% higher than given by (11). This is because of the small tilt in the spectrum which is caused by the shape of the receiver filter. The trend can be removed by subtracting two simultaneously integrated spectra from each other.

The non-random self-noise of the analyzer starts to disturb the results when the number of integrated spectra is more than 10^5.

More complete results of the test measurements are shown and discussed in detail in the original report (in finnish!) and are not repeated here.

5. SUMMARY

A real time spectrum analyzer has been designed, constructed, and tested at the EISCAT Sodankylä site. This report contains a discussion on spectrum analysis and describes the design of the analyzer. Also some test results are given.

With this report is a list of references from the original report. These references include data on subjects which have not been discussed in this report, e.g. on the use of window functions for spectral estimation and on CCD technology. Also some references on incoherent scatter and plasma line studies have been included.

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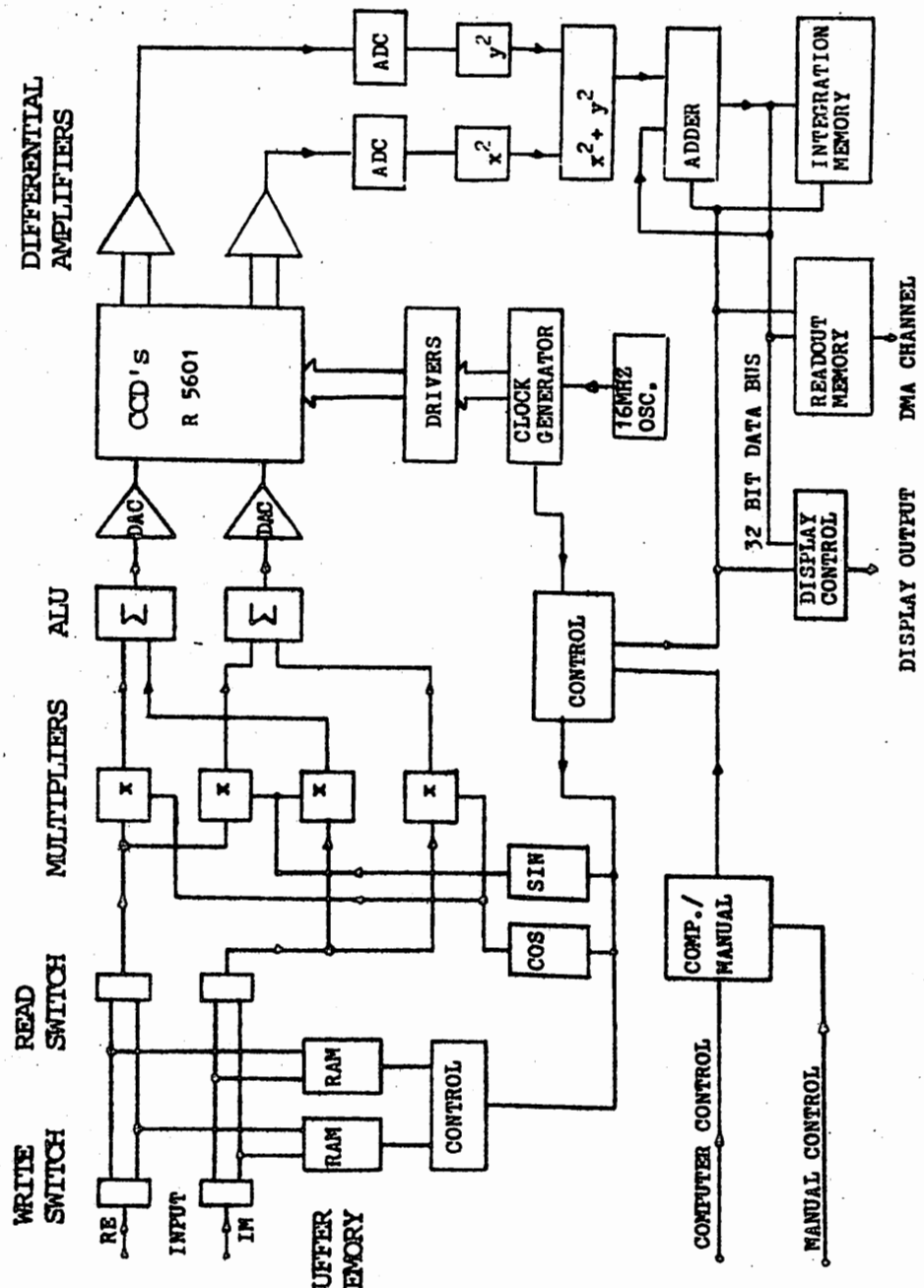


Fig. 1. SPECTRUM ANALYZER BLOCK DIAGRAM

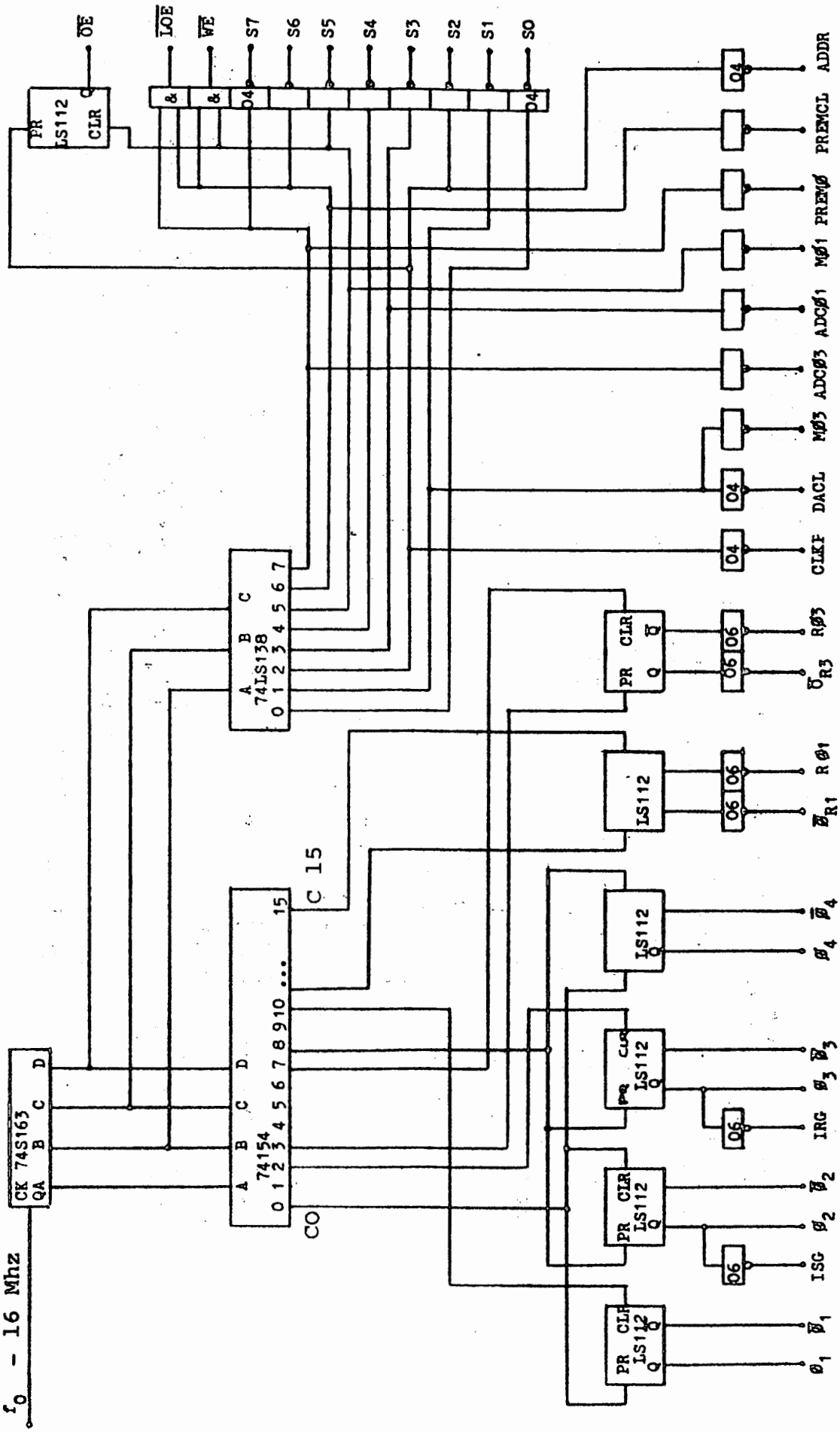


Fig.2. SPECTRUM ANALYZER CLOCK GENERATORS

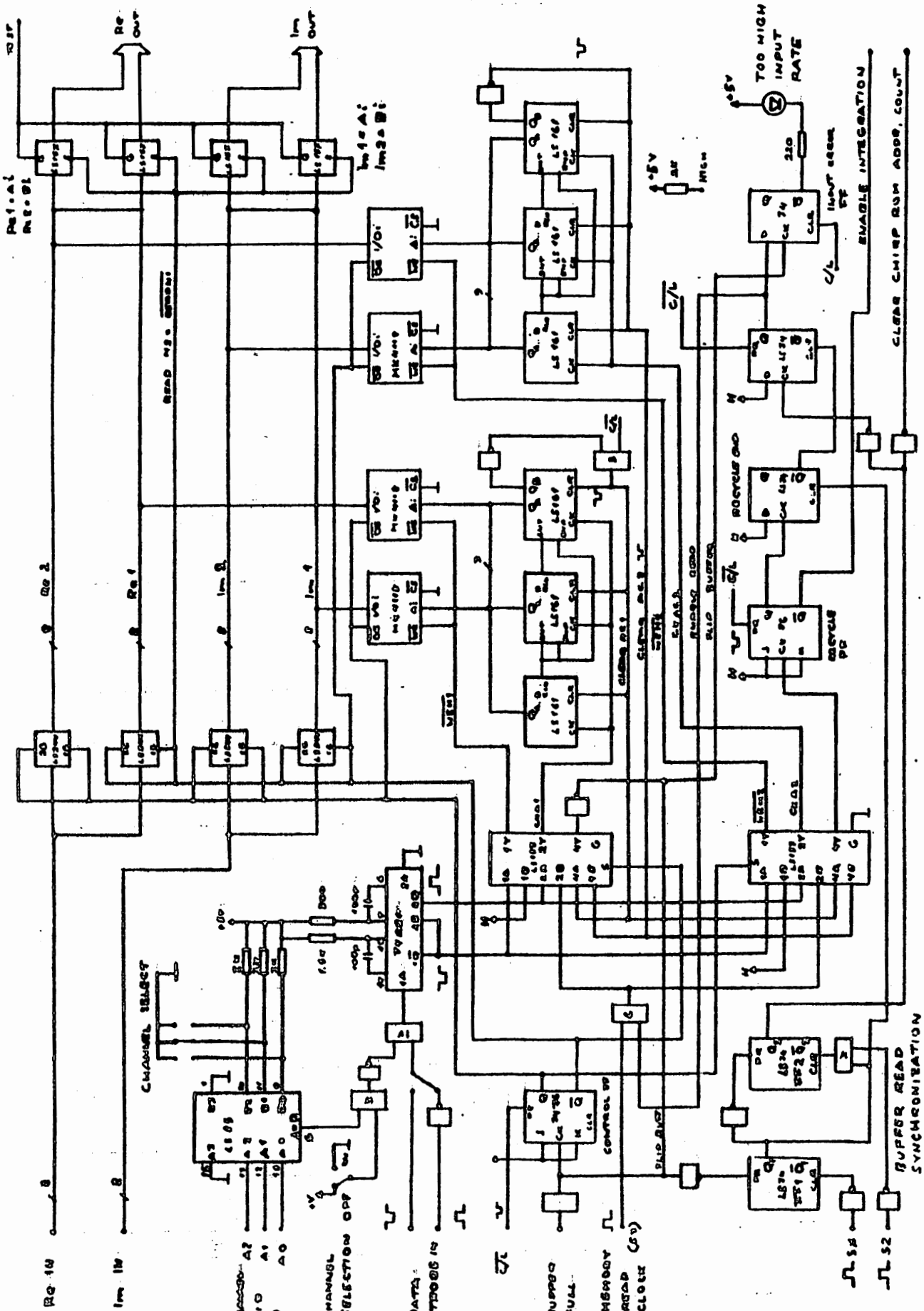
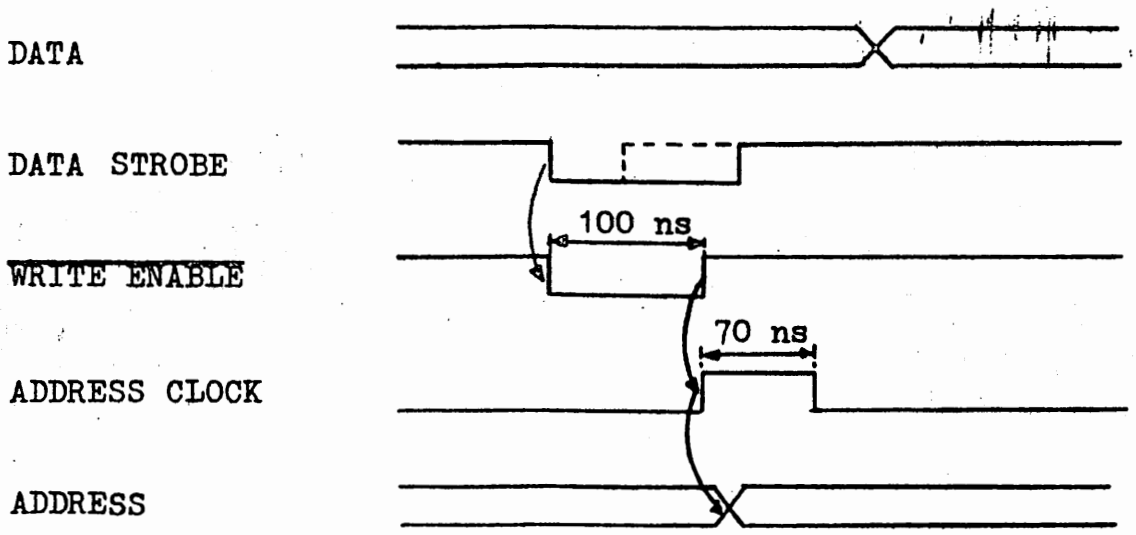
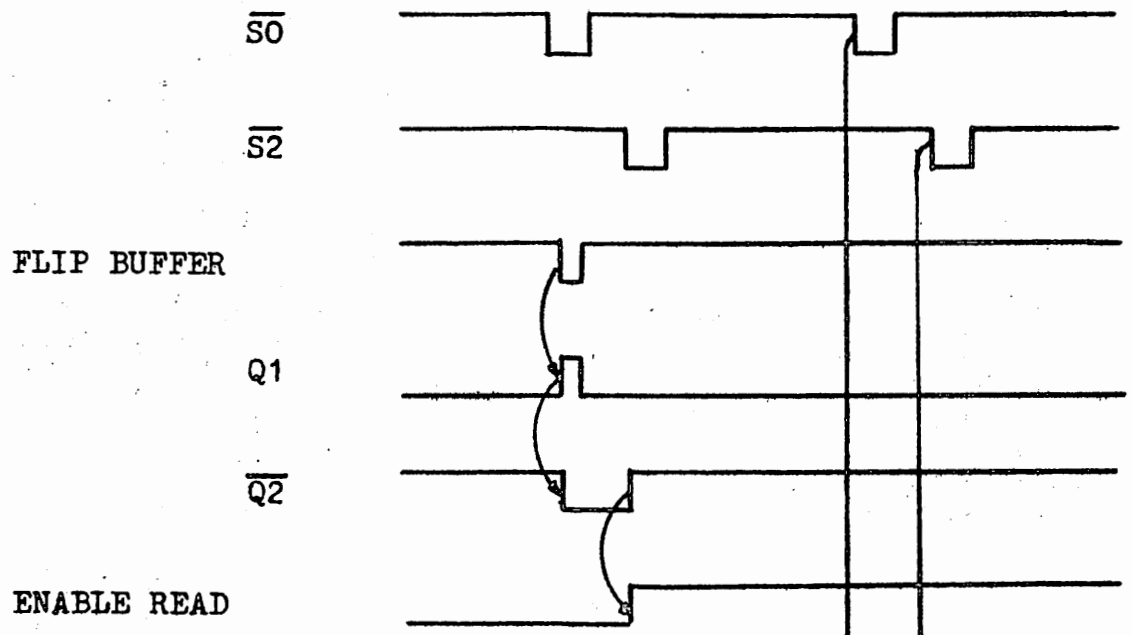


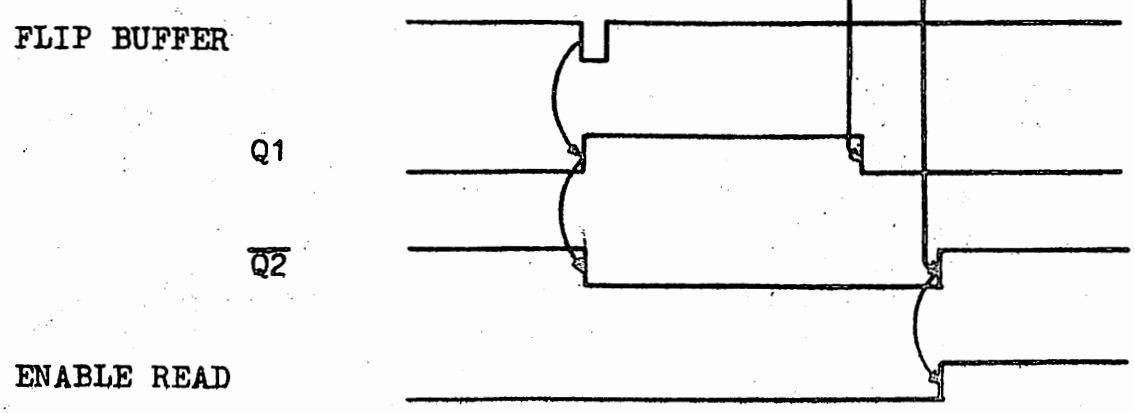
Fig. 3. SPECTRUM ANALYZER INPUT BUFFER MEMORY



BUFFER MEMORY WRITE TIMING



BUFFER READ SYNCHRONIZATION, a



BUFFER READ SYNCHRONIZATION, b

Fig. 4. BUFFER MEMORY WRITE & READ TIMING

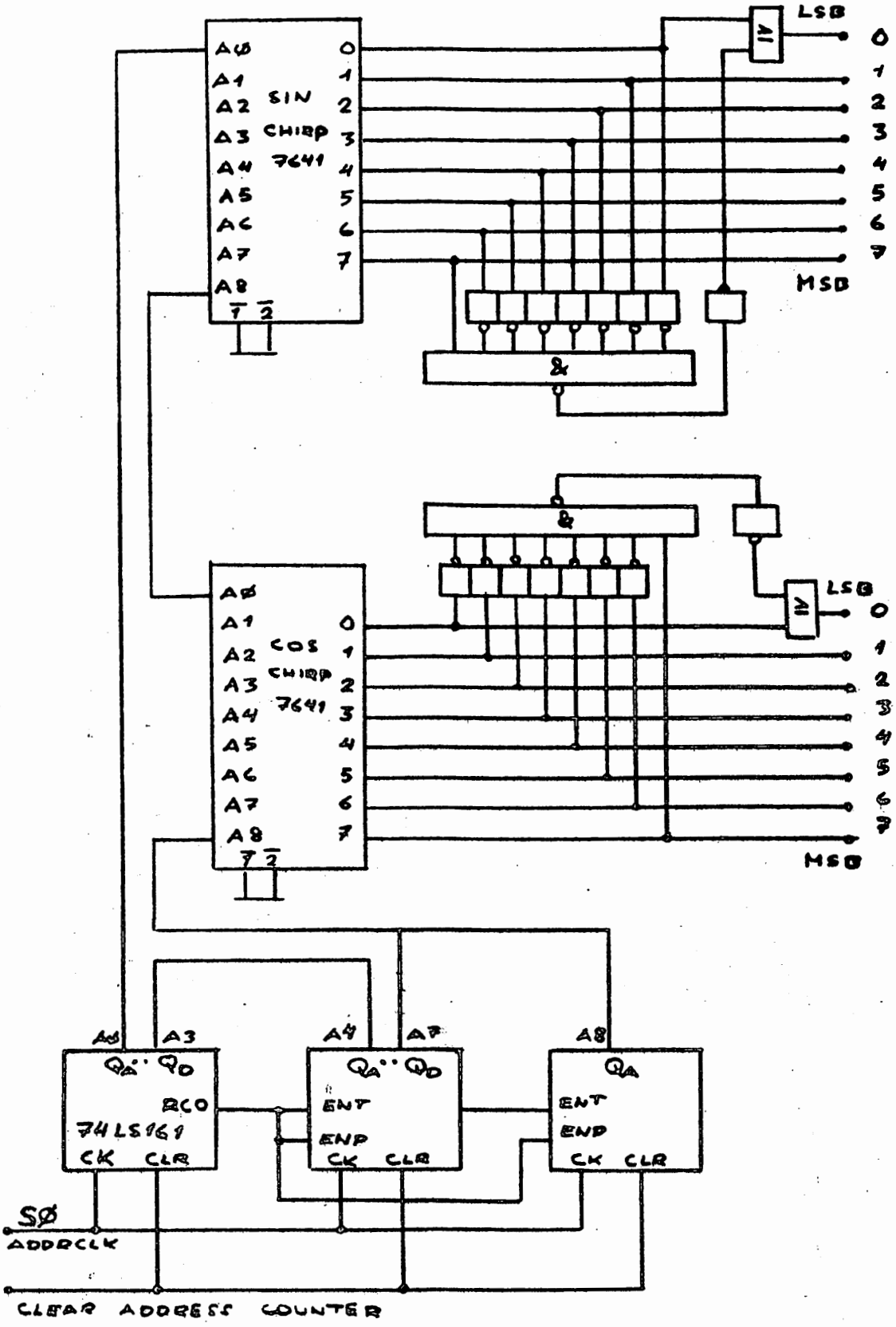


Fig. 5. PRE-CHIRP GENERATOR AND 2's COMPLEMENT MODIFICATION

80-10-30 /TK

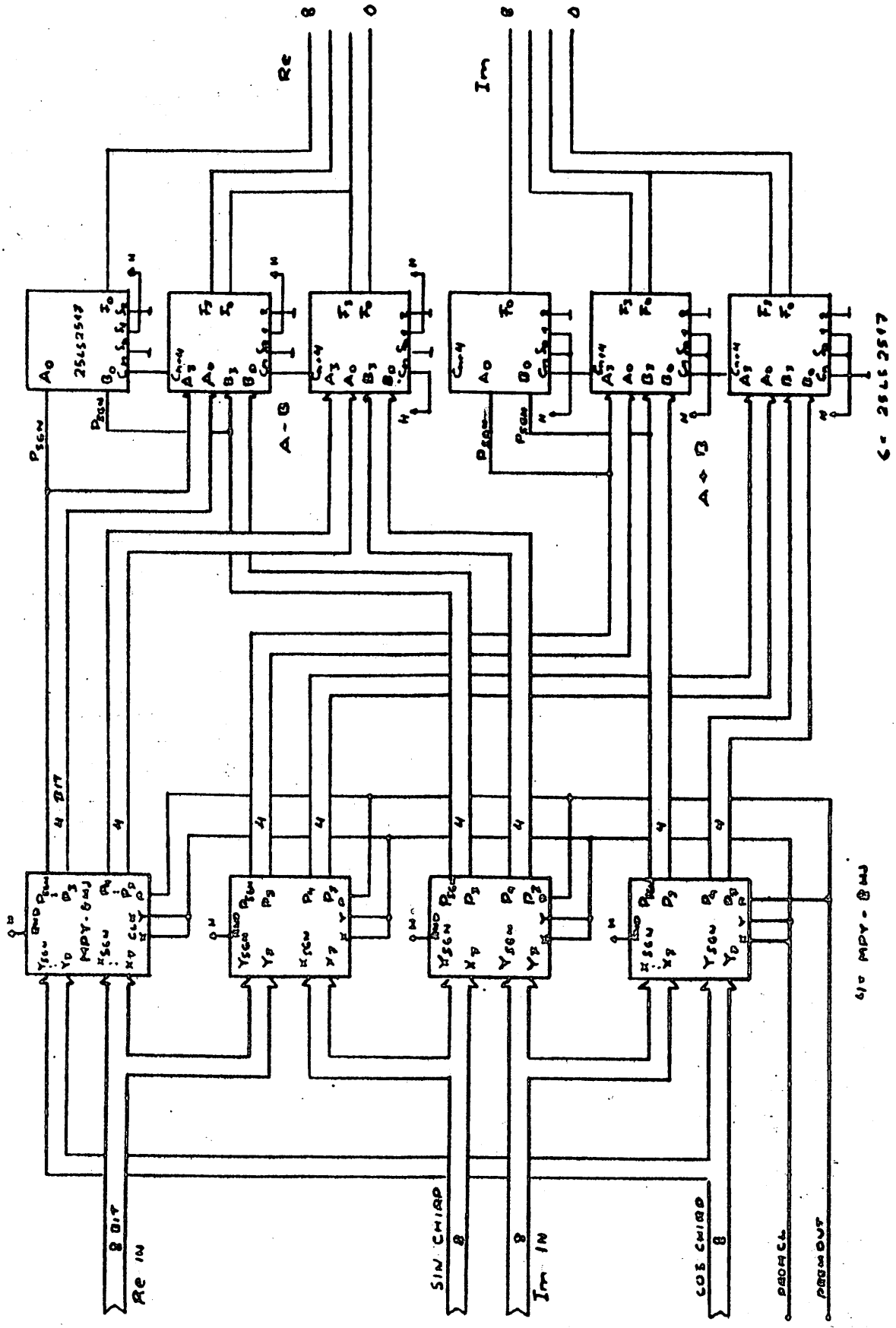


Fig. 6. SPECTRUM ANALYZER PREMULTIPLIERS

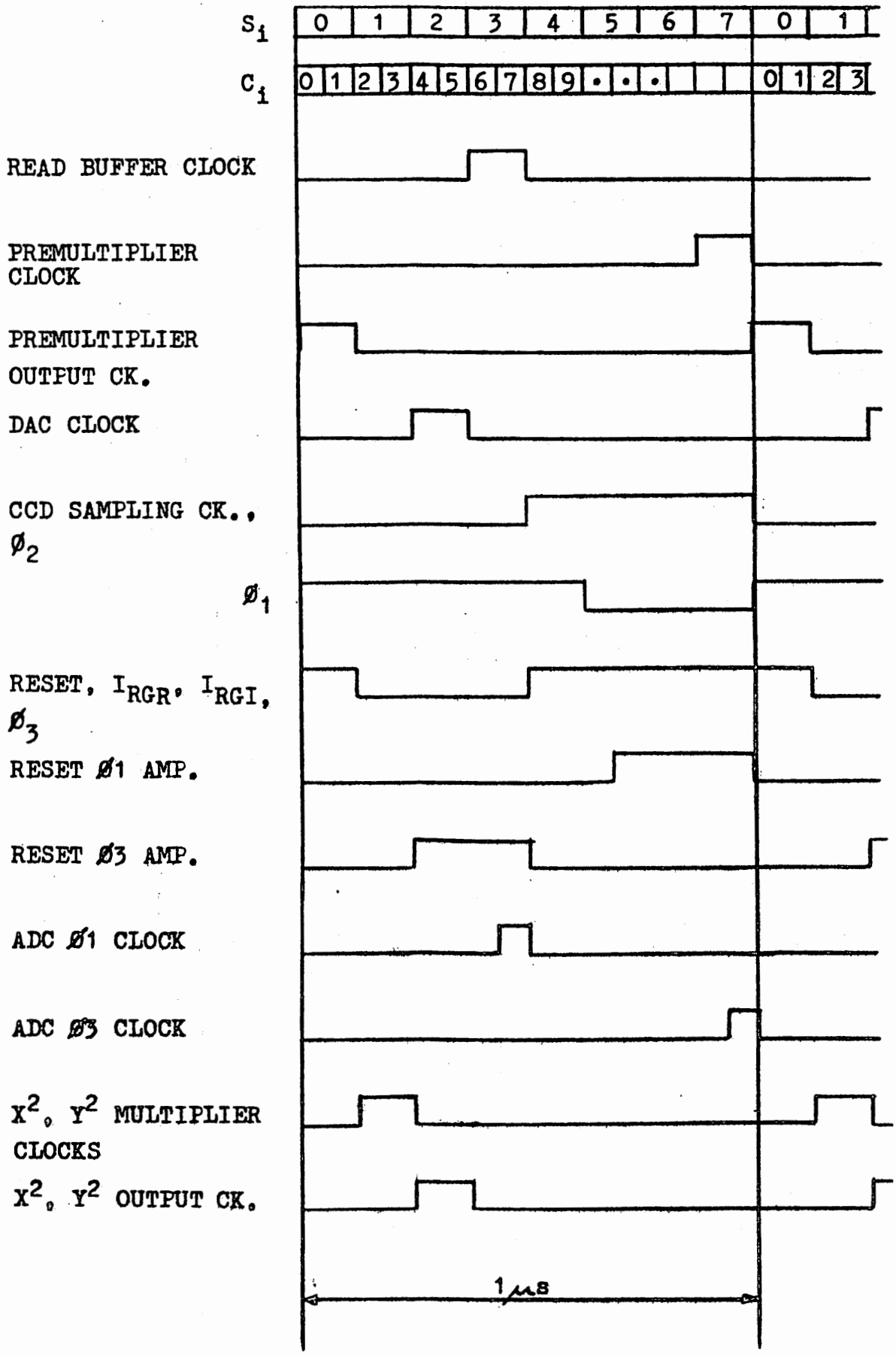


Fig. 7. SYNCHRONOUS PART TIMING I.

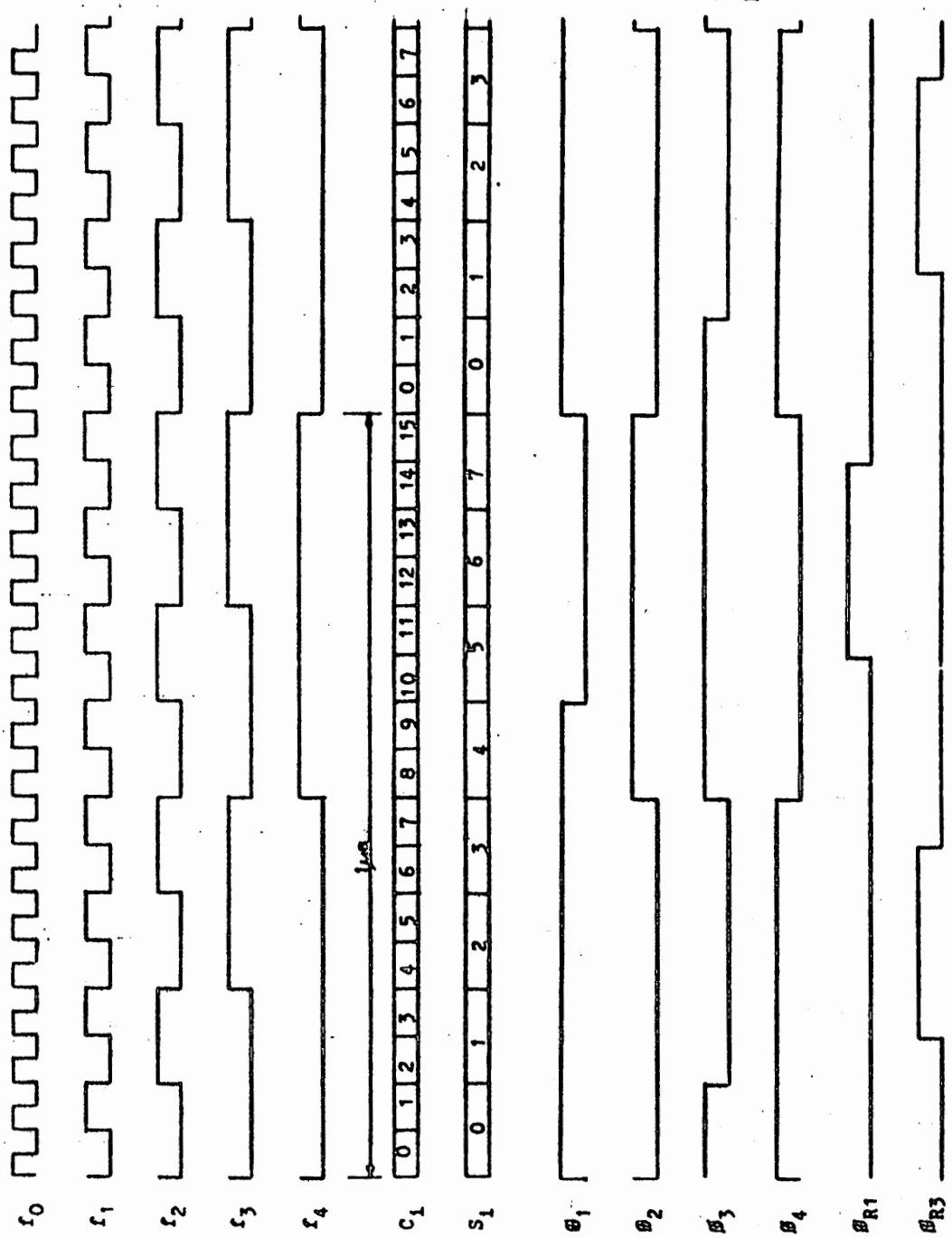


Fig 8. CCD TIMING

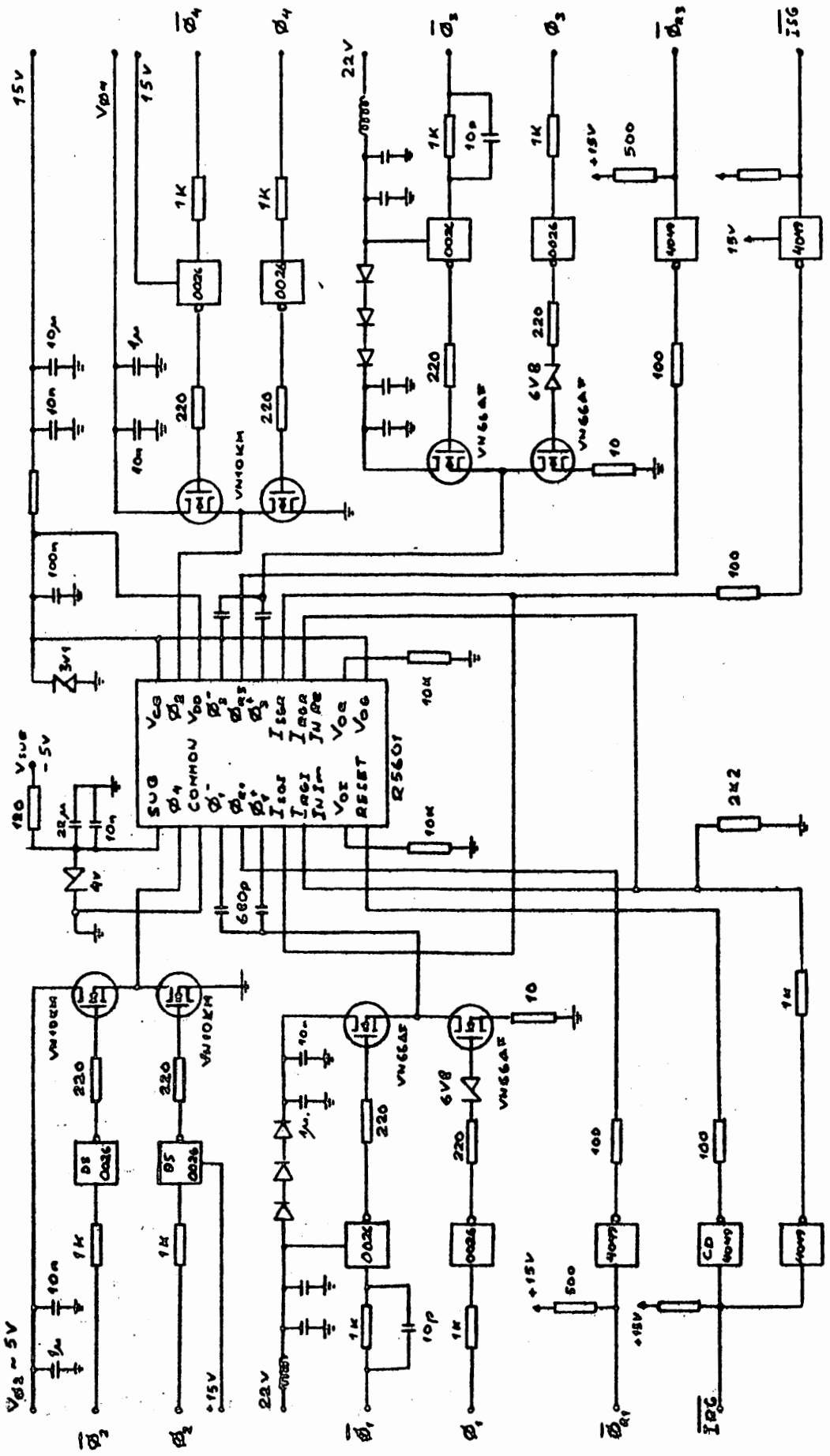


Fig. 9. SPECTRUM ANALYZER CCD CLOCK DRIVERS

80-10-16

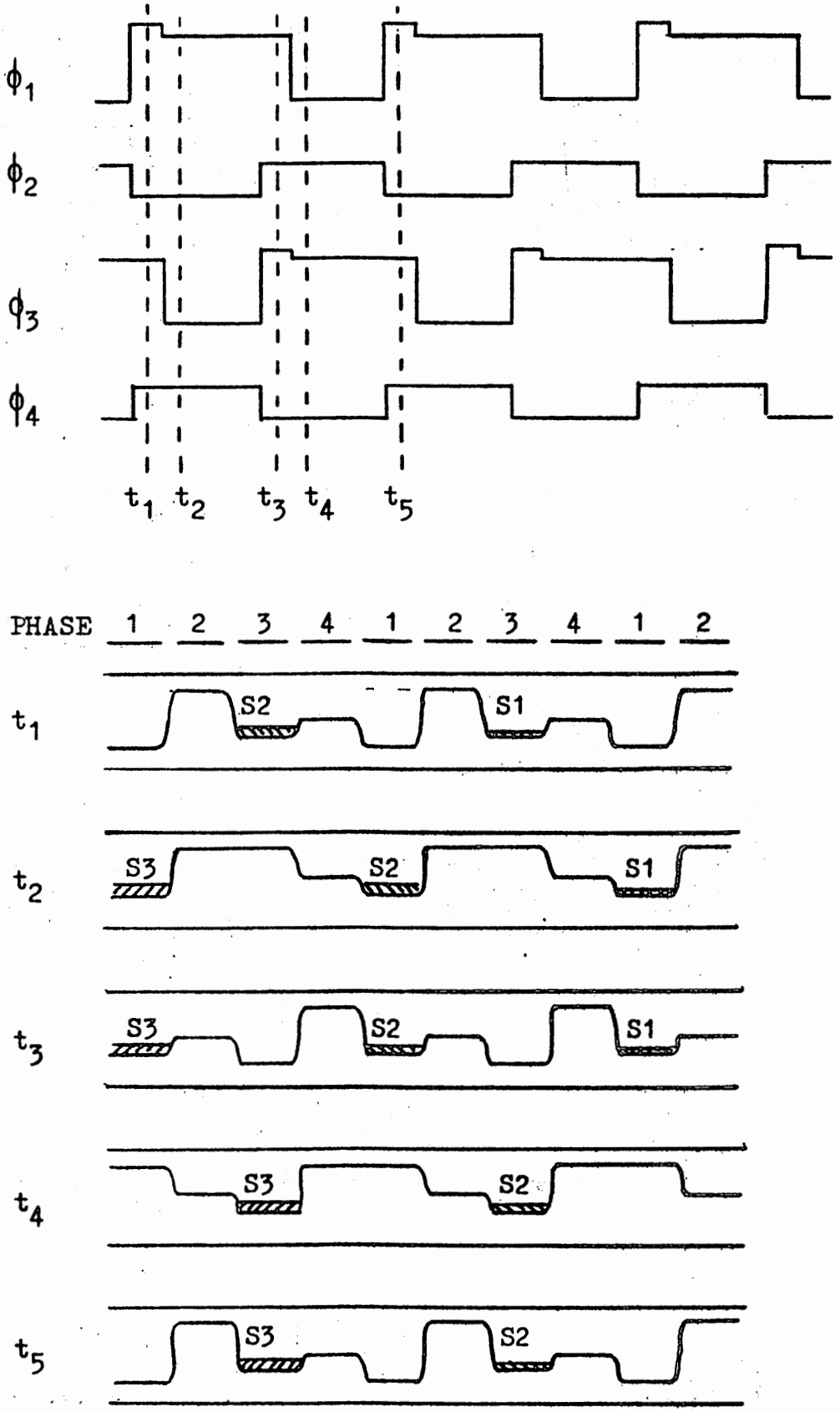


Fig. 10. Schematic illustration of the charge transfer in R5601.

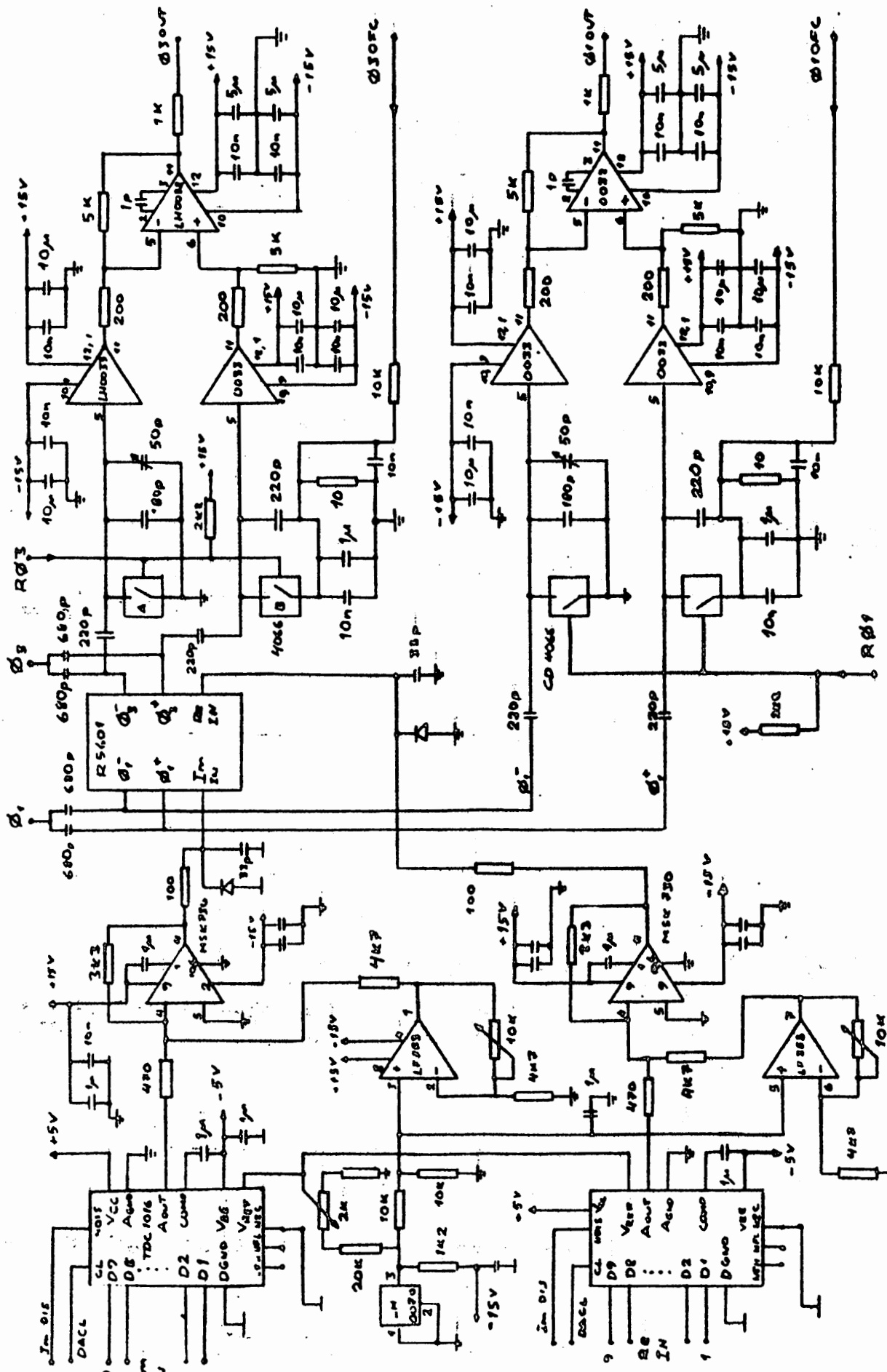


Fig. 11. SPECTRUM ANALYZER CCD INPUT AND SIGNAL EXTRACTION

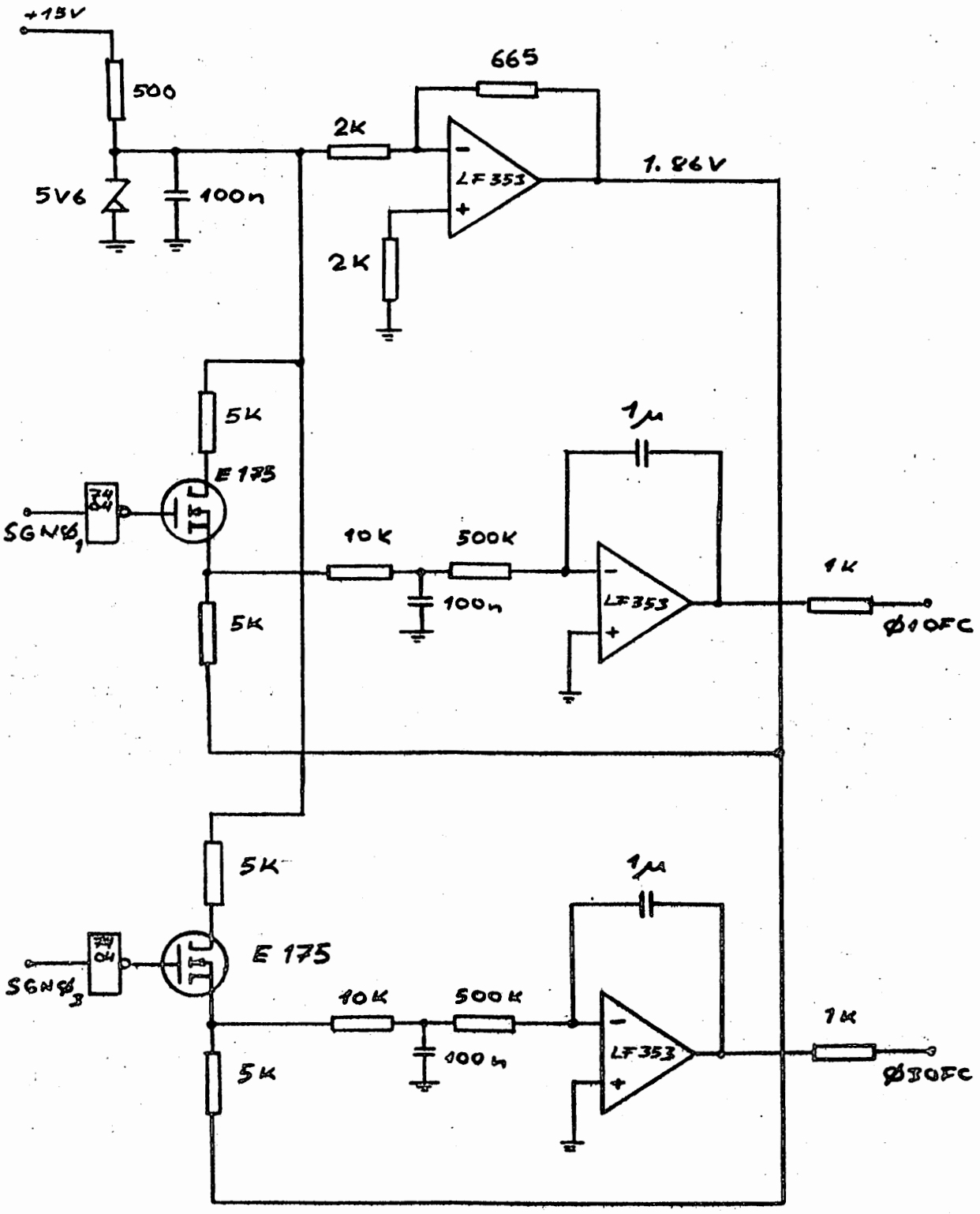


Fig. 12. SPECTRUM ANALYZER READOUT AMPLIFIER OFFSET COMPENSATION

81-01-23 /TA

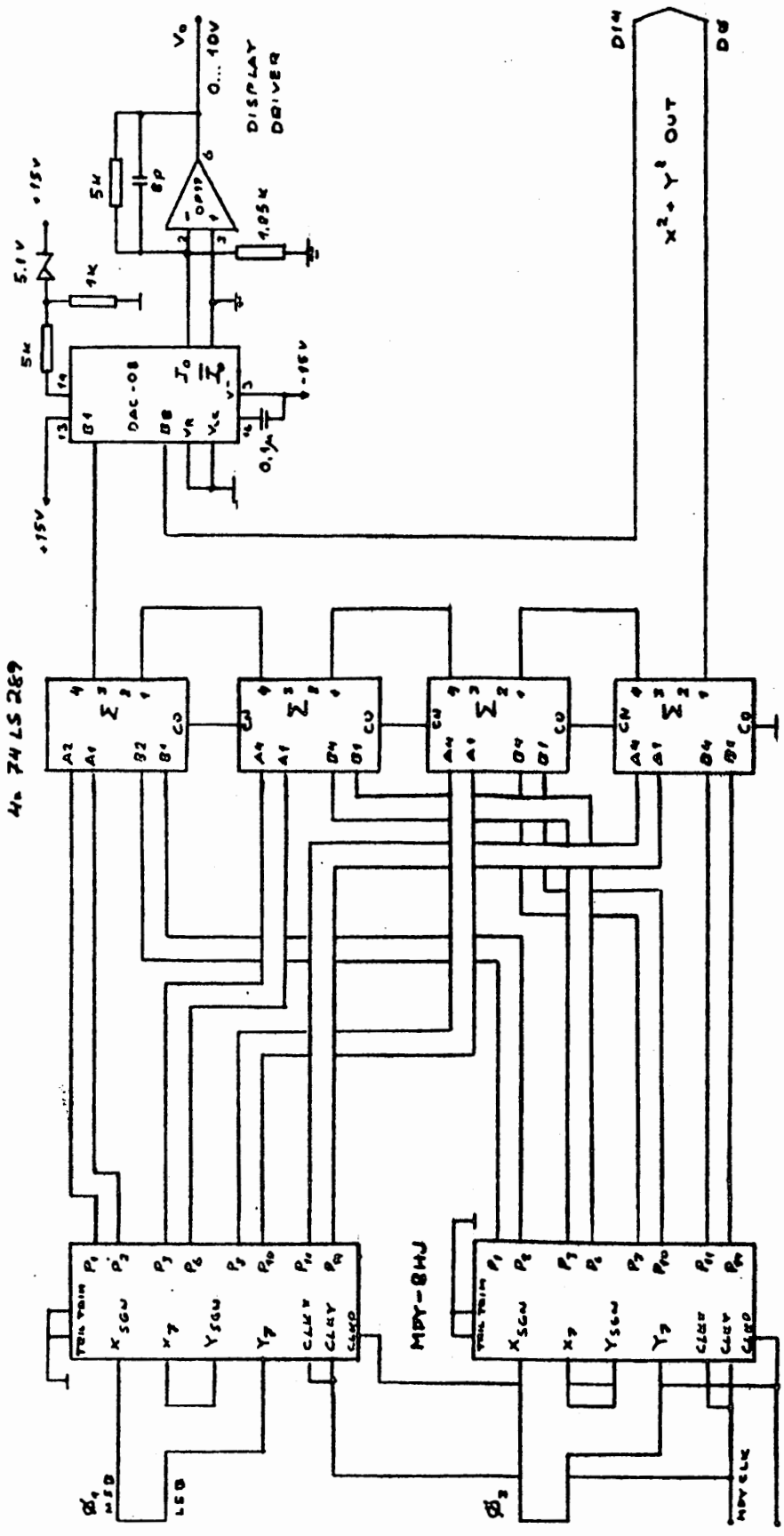


Fig. 13. SPECTRUM ANALYZER POWER COMPUTATION

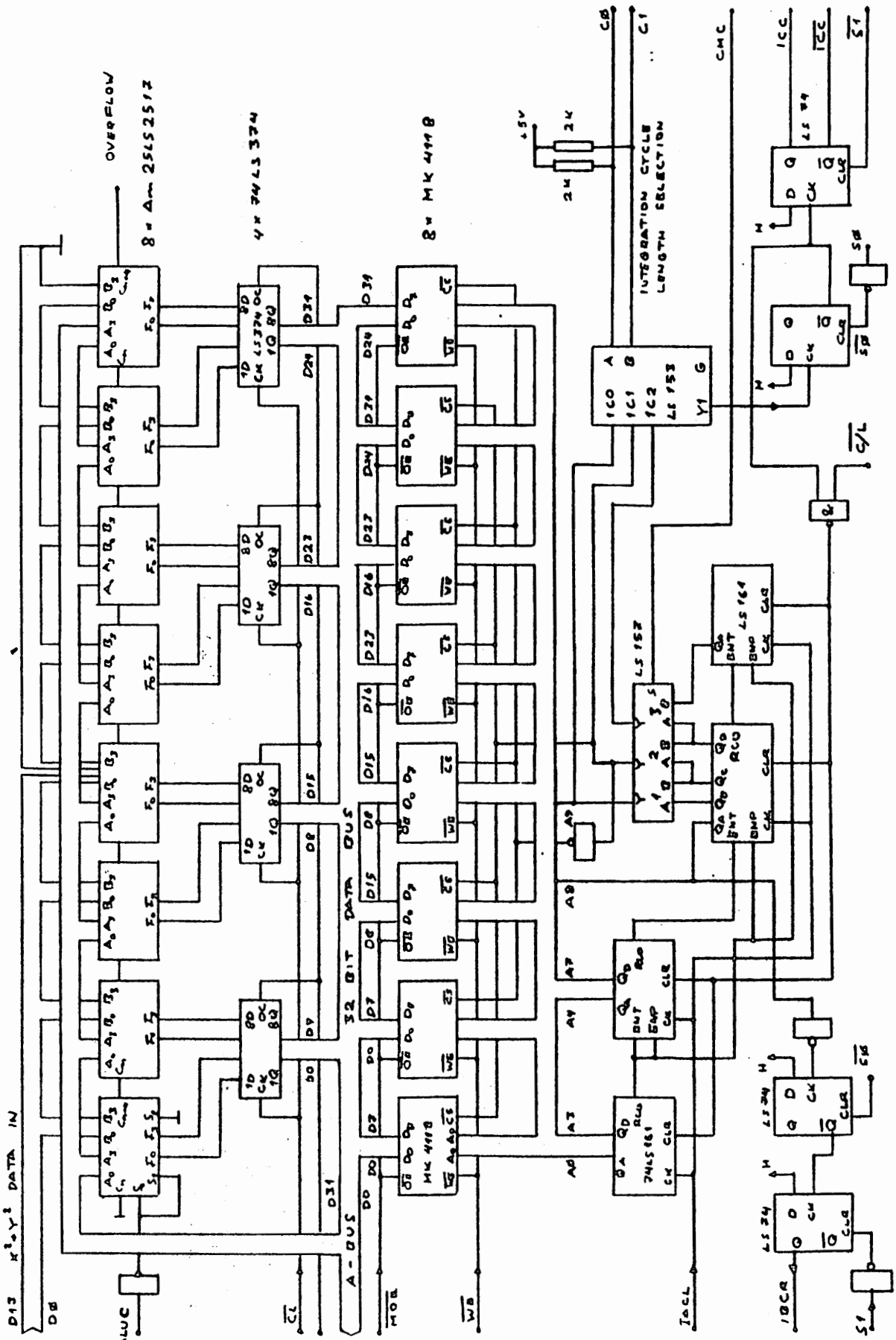


Fig. 14. SPECTRUM ANALYZER INTEGRATOR

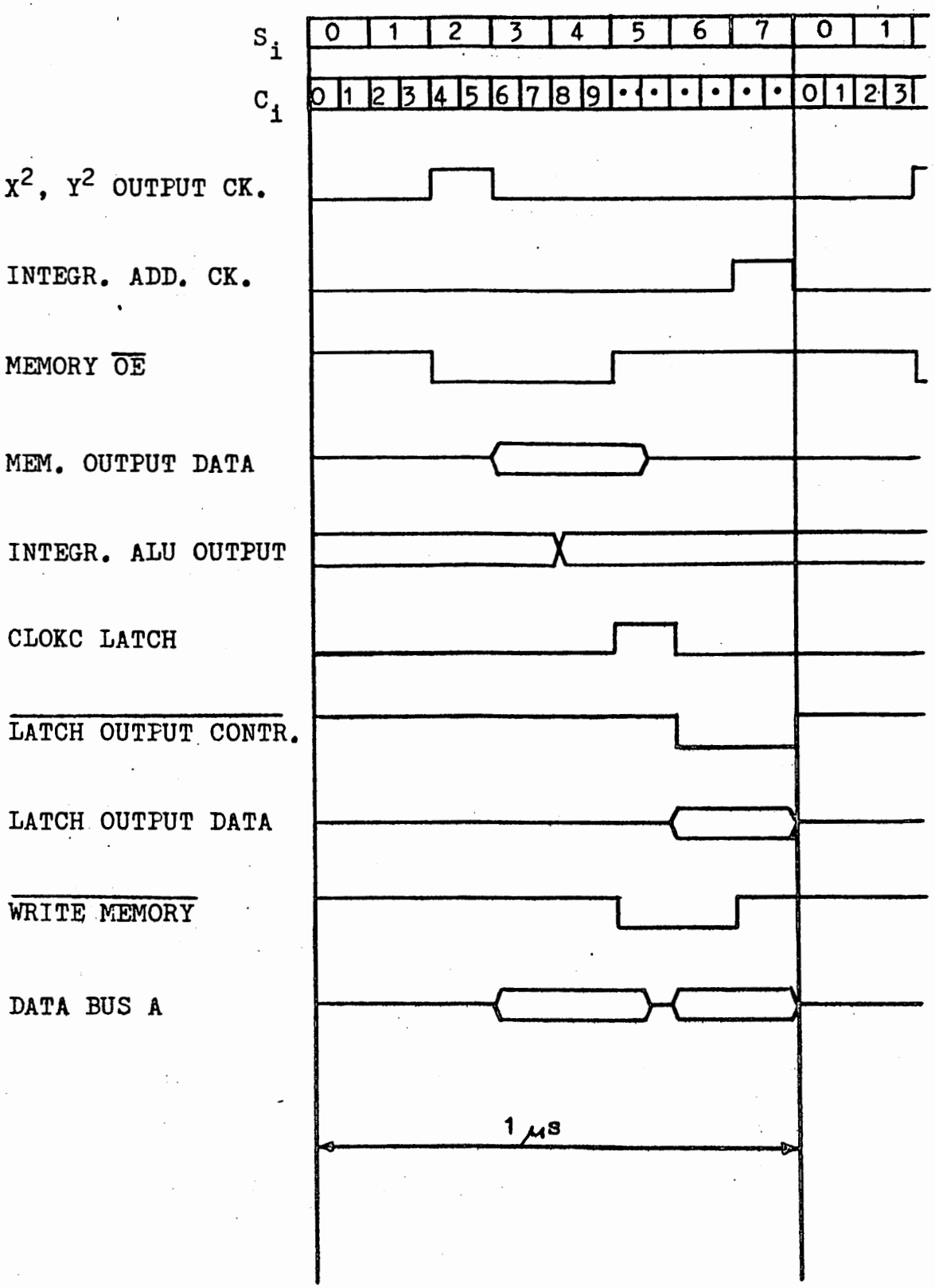


Fig. 15. SYNCHRONOUS PART TIMING II, INTEGRATOR.

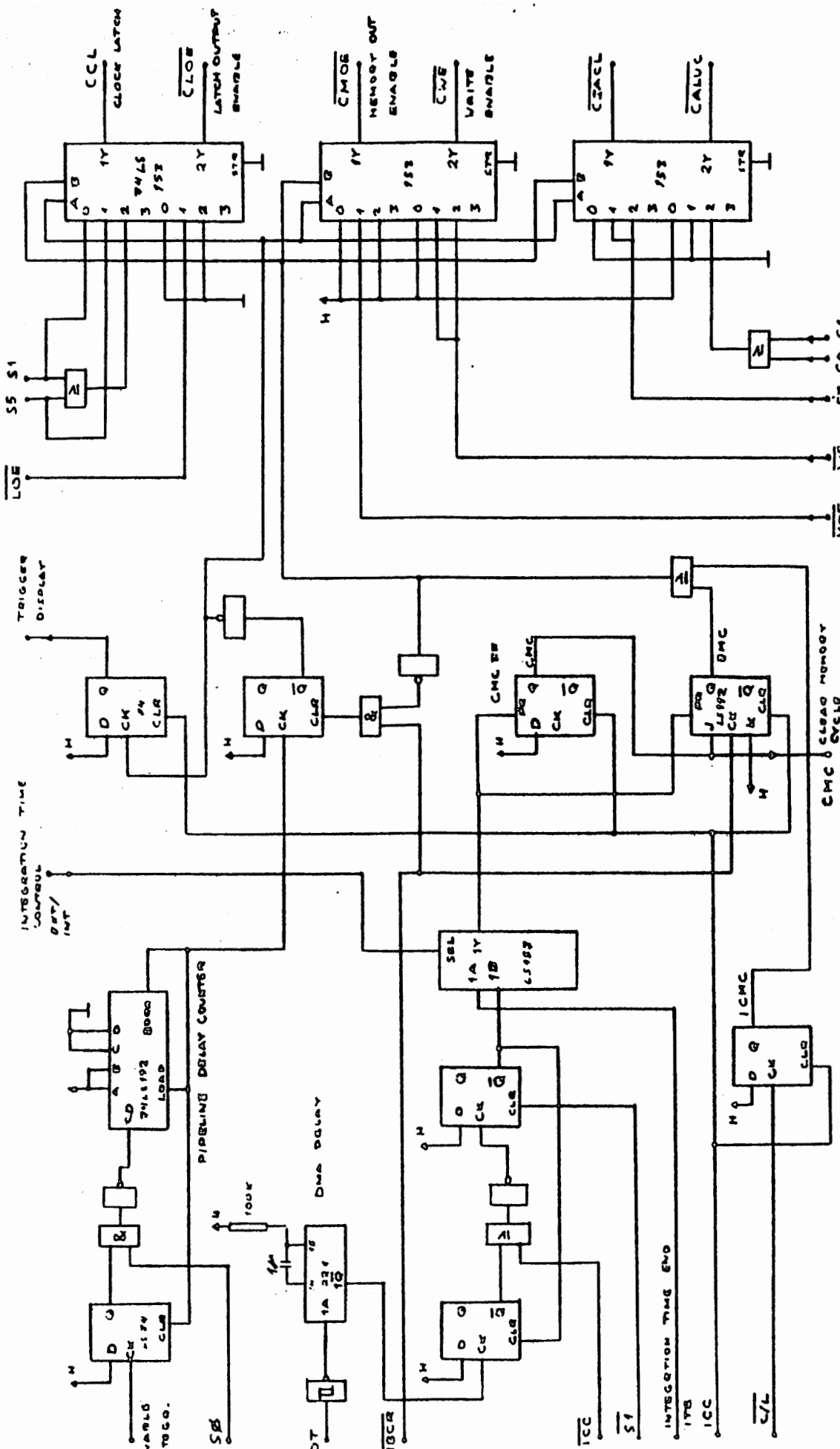


Fig 16. SPECTRUM ANALYZER INTEGRATOR AND READOUT CONTROL

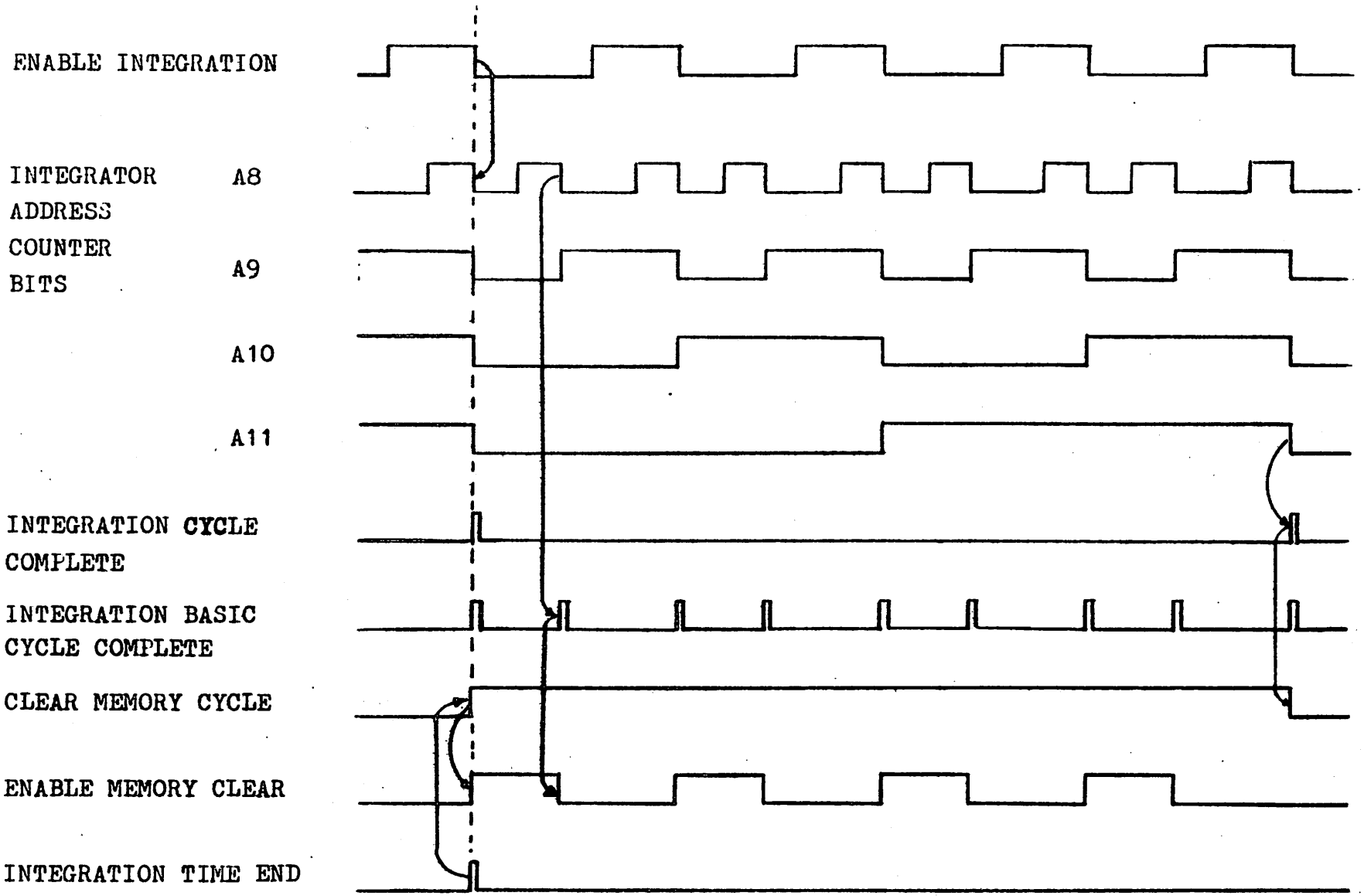


Fig. 17. INTEGRATOR CLEAR TIMING

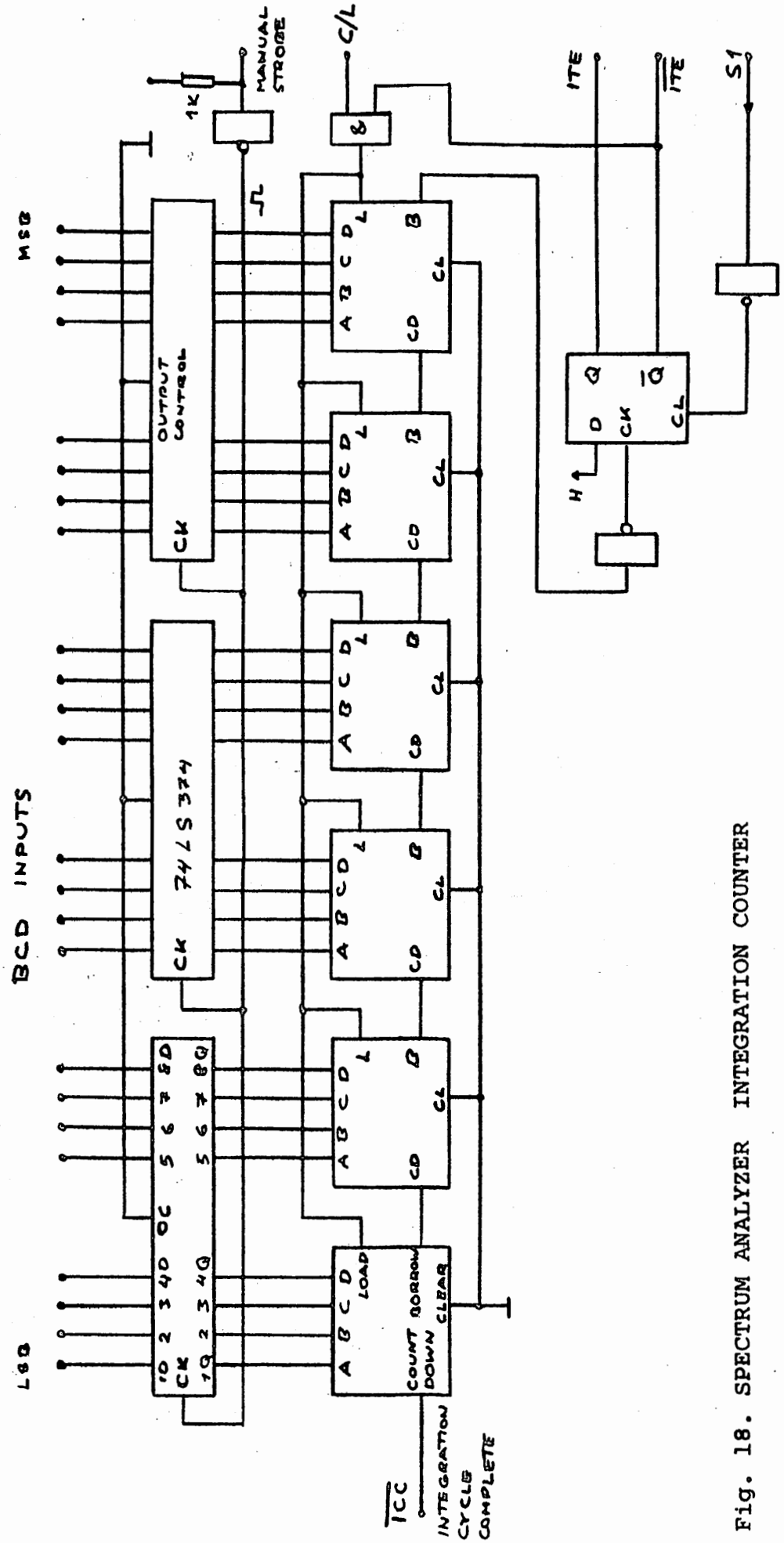


Fig. 18. SPECTRUM ANALYZER INTEGRATION COUNTER

81-01-28/78

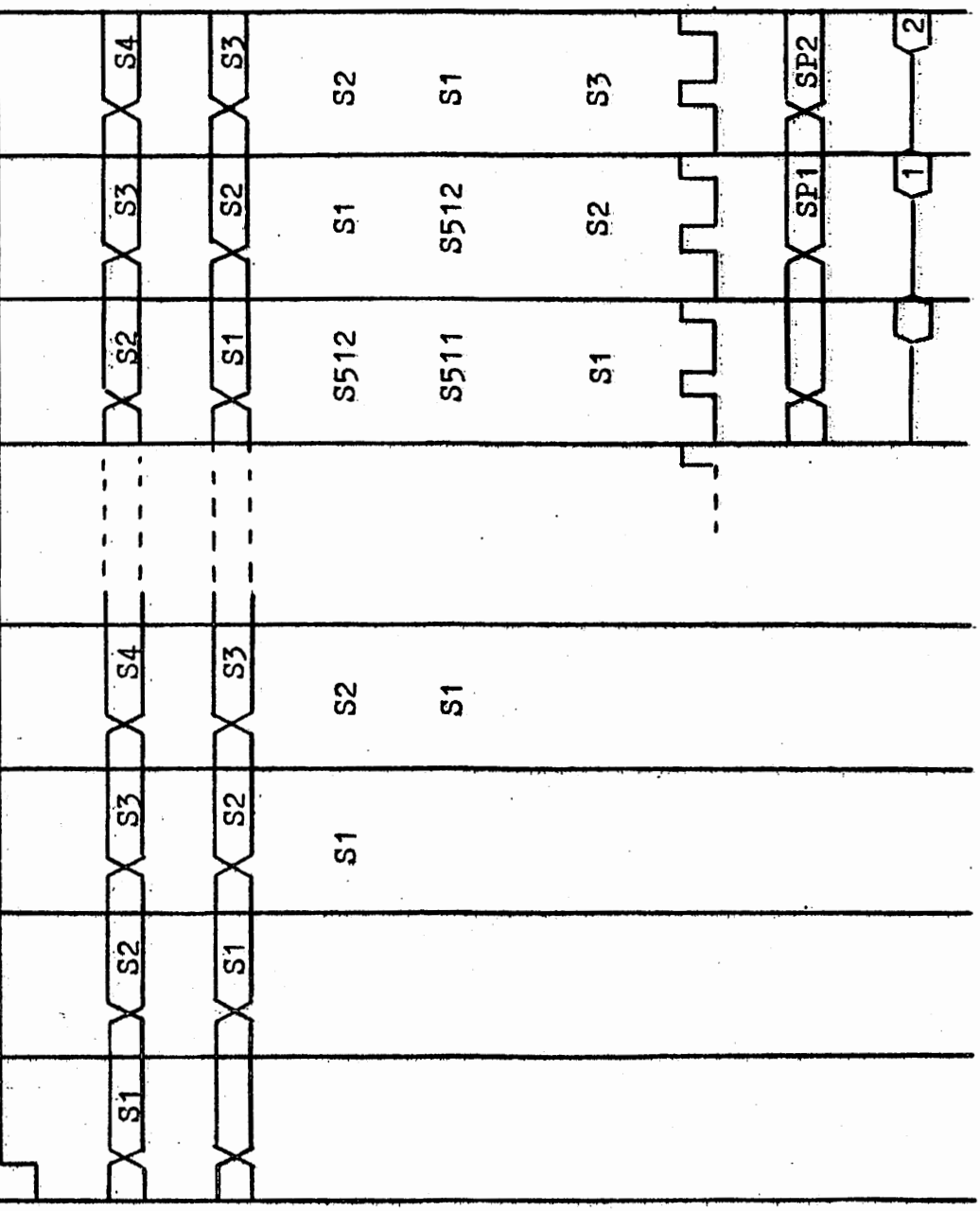


Fig. 19. SPECTRUM ANALYZER DELAY DIAGRAM

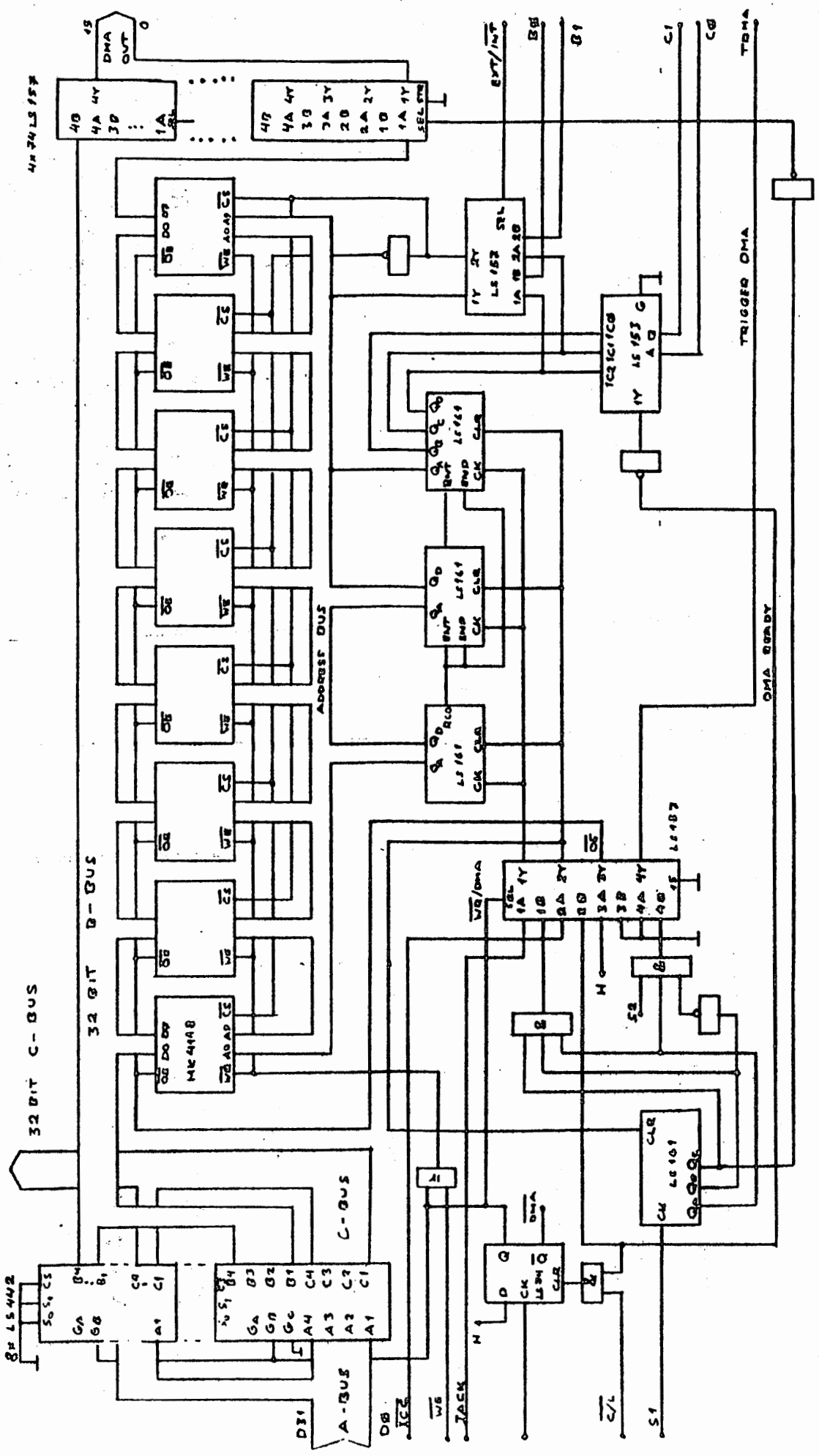


Fig. 20. SPECTRUM ANALYZER READOUT MEMORY

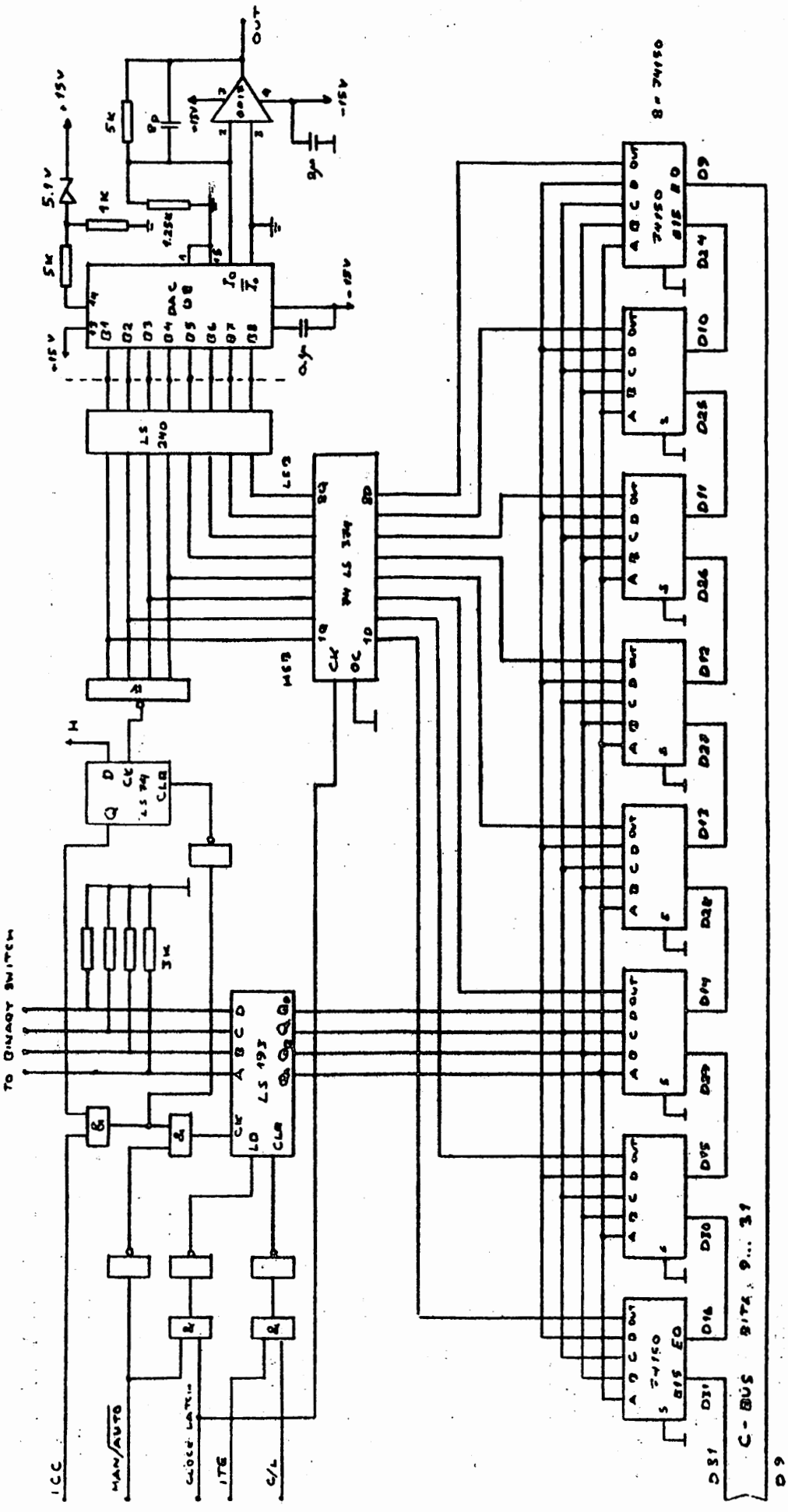


Fig. 21. SPECTRUM ANALYZER DISPLAY CONTROL

1981-02-12/K

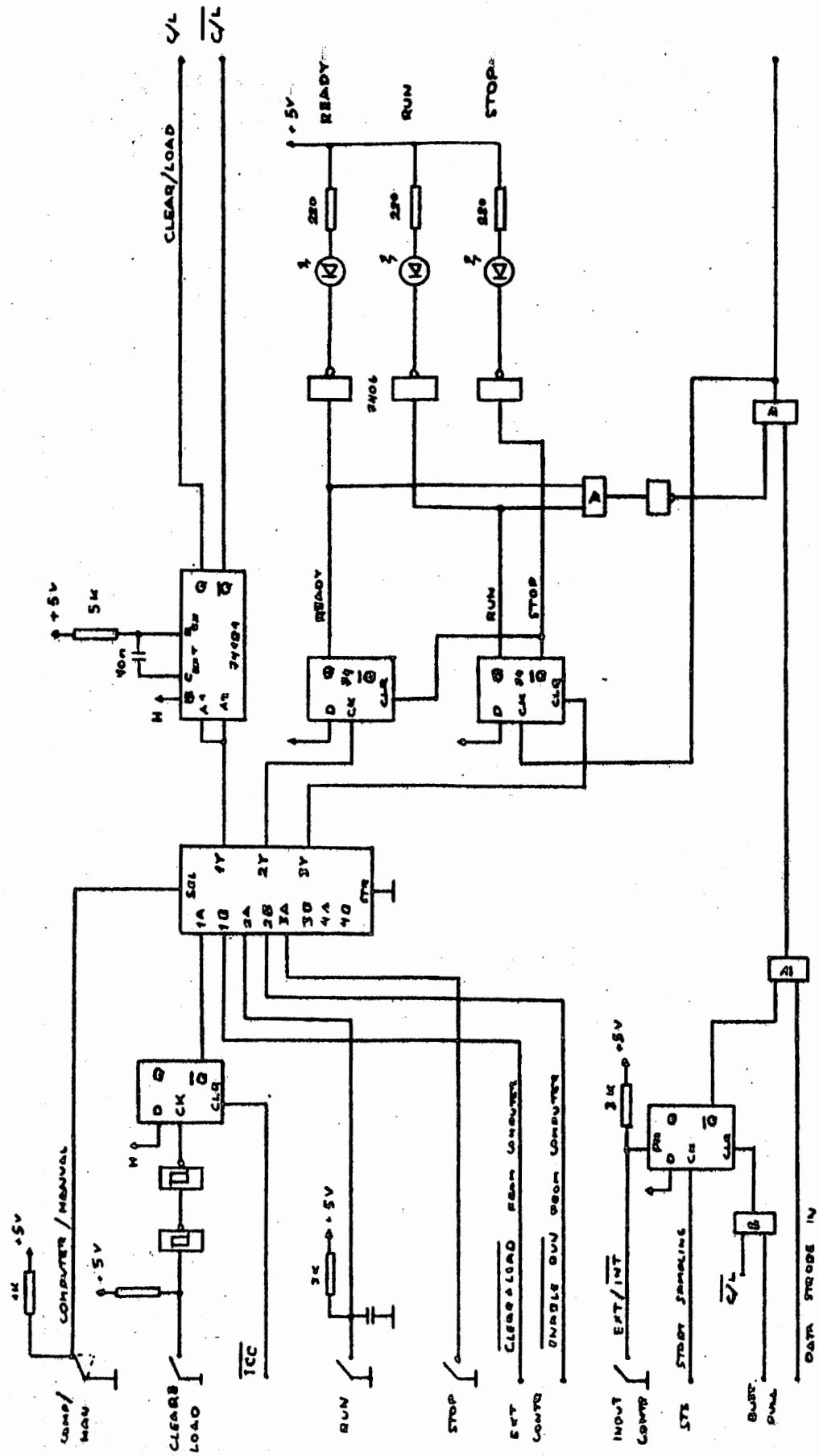


Fig. 22. SPECTRUM ANALYZER OPERATION CONTROL

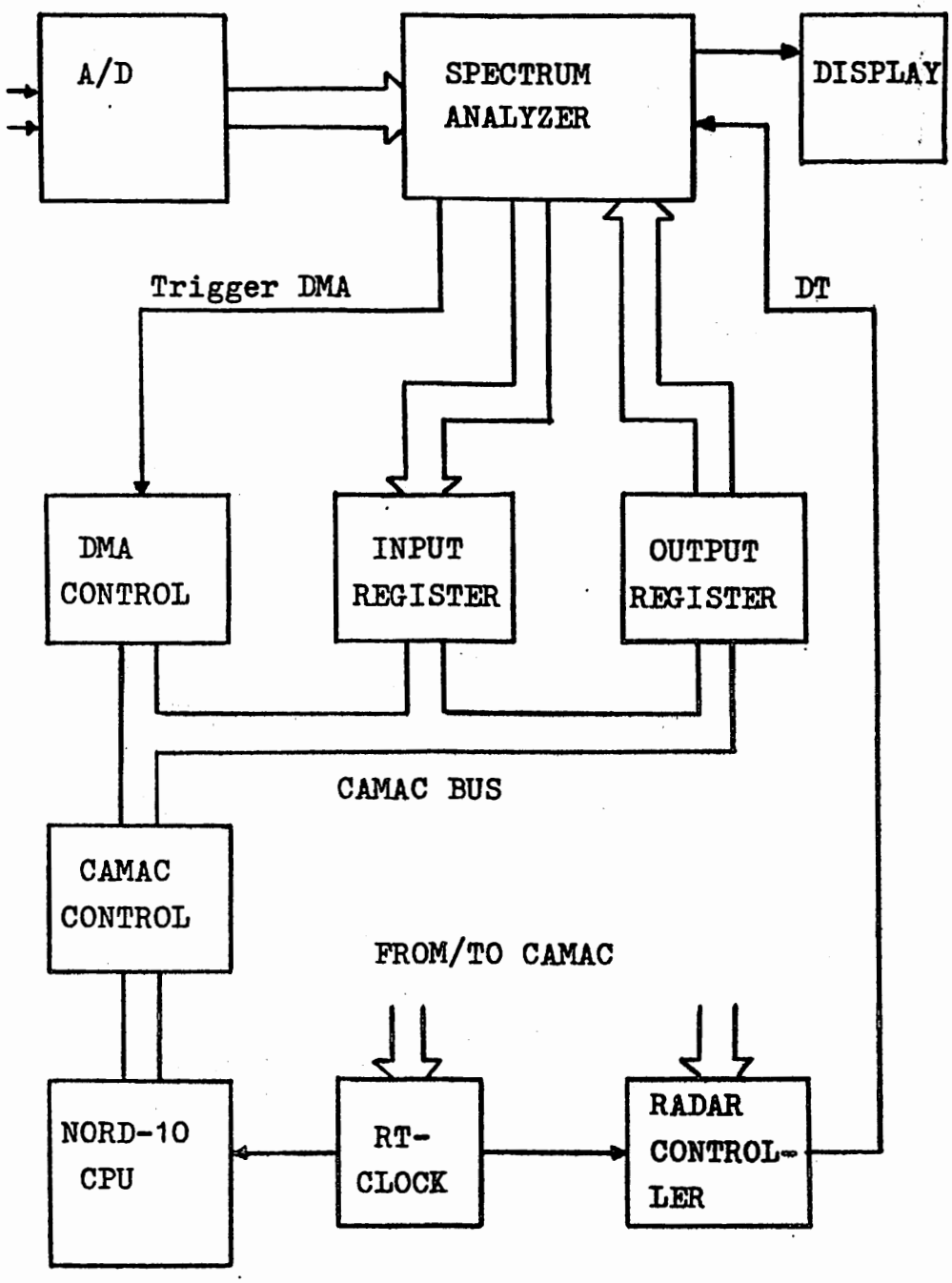
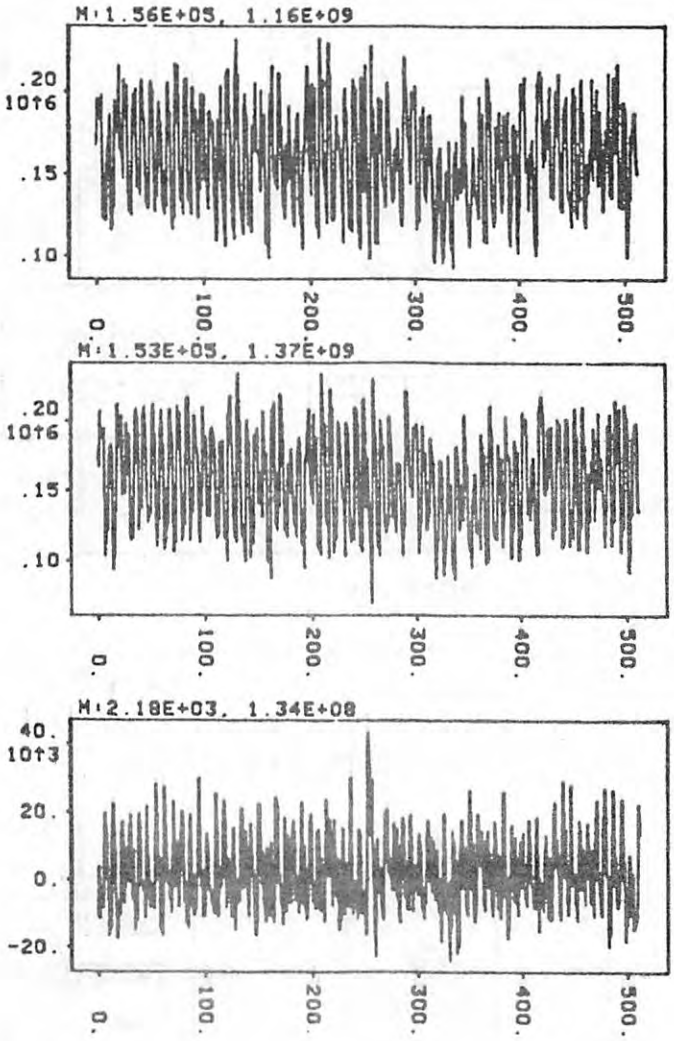
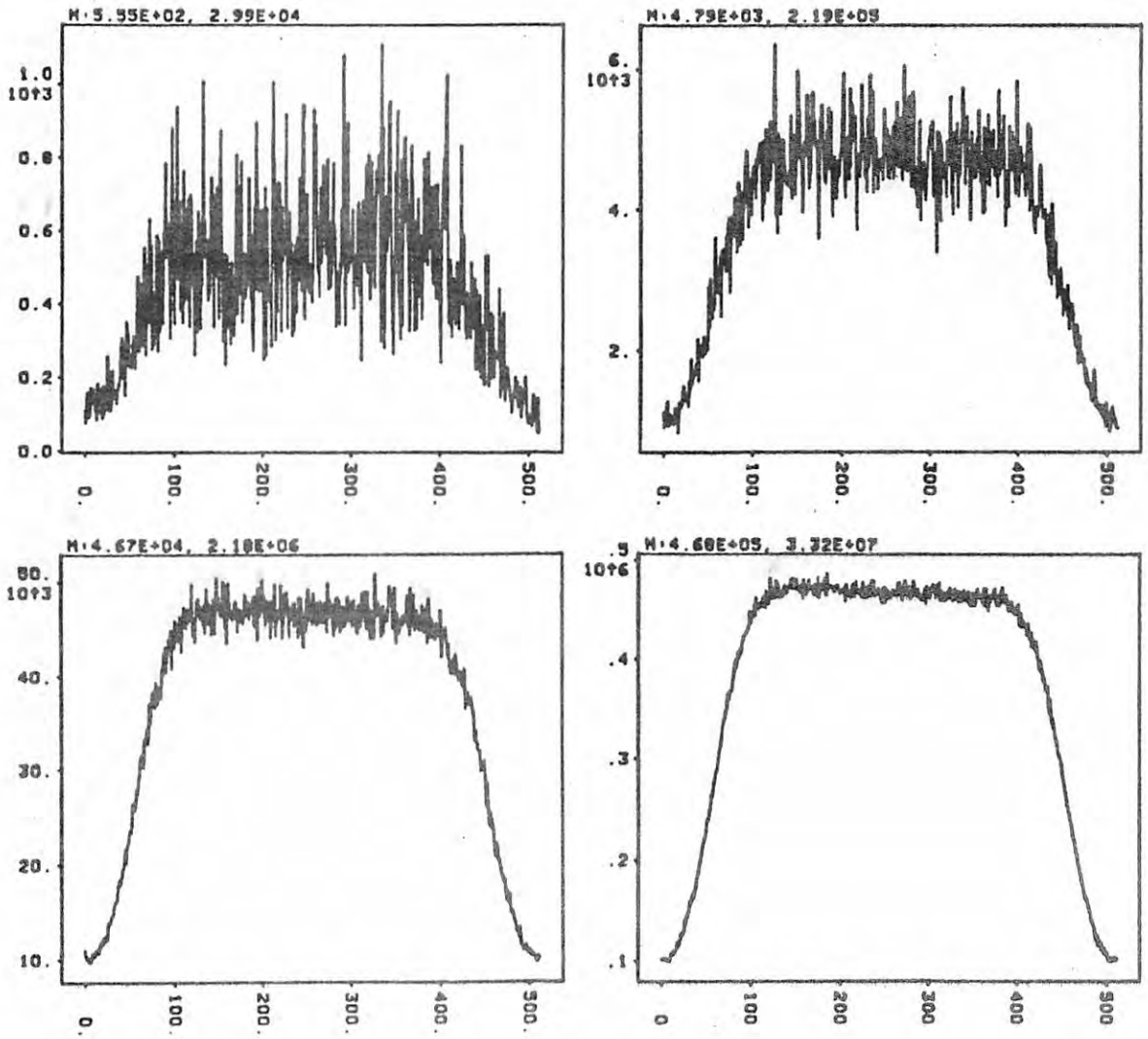


Fig. 23. SPECTRUM ANALYZER INTERFACE WITH EISCAT RECEIVING SYSTEM



At the top and in the middle there are two simultaneously integrated spectra S_{N1} and S_{N2} of the noise generated by the analyzer. At the bottom is the result of the subtraction, $S_{N1}-S_{N2}$. The number of spectra (N) is 1.4×10^5 and the average of 200 spectral points is 1.56×10^5.

Fig. 24



N	S_N	S_N^2/N	var(S_N)
10	$5.55\ 10^2$	$3.08\ 10^4$	$2.99\ 10^4$
10^2	$4.79\ 10^3$	$2.29\ 10^5$	$2.19\ 10^5$
10^3	$4.67\ 10^4$	$2.18\ 10^6$	$2.18\ 10^6$
10^4	$4.68\ 10^5$	$2.19\ 10^7$	$3.32\ 10^7$

Spectra of external noise. Number N of added spectra is 10, 100, 1000 and 10 000. The results of the calculations are shown below the figures. Above each figure there is the mean of 200 points in the middle of the spectrum and the variance calculated from the same points.

fig. 25.